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CPLD BASED CONTROL SYSTEM OF THE THREE-PHASE ZERO-CURRENT-TRANSITION INVERTER

Układ sterowania przekształtnika trójfazowego przełączanego w warunkach zerowego prądu, zbudowany na bazie struktur programowych

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Summary: **This paper presents design, analysis and practical realisation of the control system for the three phase six –switch ZCT inverter. Complete design procedure for high power soft switching inverter is shown. Selection of the resonant tank elements and their influence on the control signals are discussed. Control algorithm was implemented in to CPLD device (Complex Programmable Logic Devices). Individual control blocks and their functions are described.**

Streszczenie :**Prezentowana praca dotyczy zagadnień projektowania, analizy i realizacji praktycznej układu sterowania trójfazowego przekształtnika rezonansowego przełączanego w warunkach zerowego prądu –ZCT. Przedstawiono zasady doboru wartości elementów obwodu rezonansowego oraz zależności czasowe dla sygnałów sterujących przekształtnik. Zaprezentowano przykład realizacji praktycznej układu sterowania w oparciu o układy logiki programowalnej typu CPLD.**

Key words: resonant inverter, soft switching, ZCT
Słowa kluczowe: przekształtnik rezonansowy, miękka komutacja, ZCT

1. INTRODUCTION

The ZCT technique enables to reduce the switching turn-off losses in the power transistors of an inverter. Additional switches and resonant tanks are required. One of the best efficiency, about 97%, is achieved with ZCT six –switch inverter topology [1]. Additionally, this kind of the inverter may be controlled by PWM type modulation. Figure 1 displays the six –switch ZCT inverter.

The operational waveforms during one switching cycle, in one leg of the inverter, when load current I>0, are illustrated in Fig. 2.

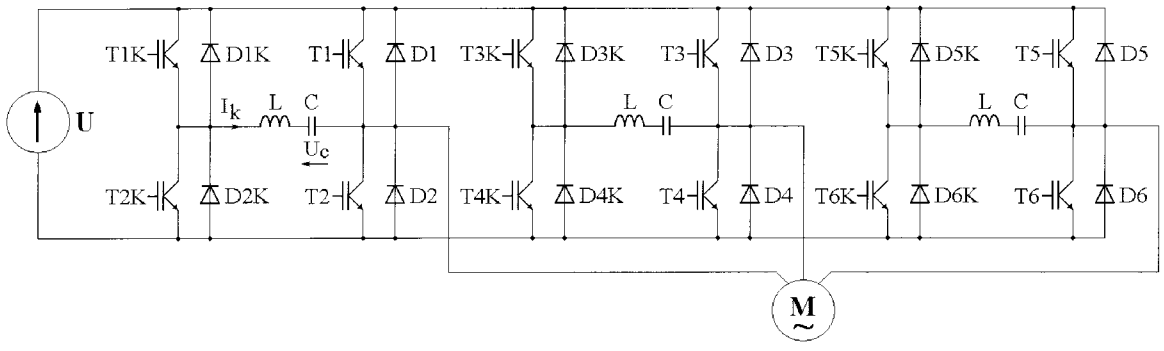

Fig. 1. The ZCT three-phase inverter with six auxiliary switches

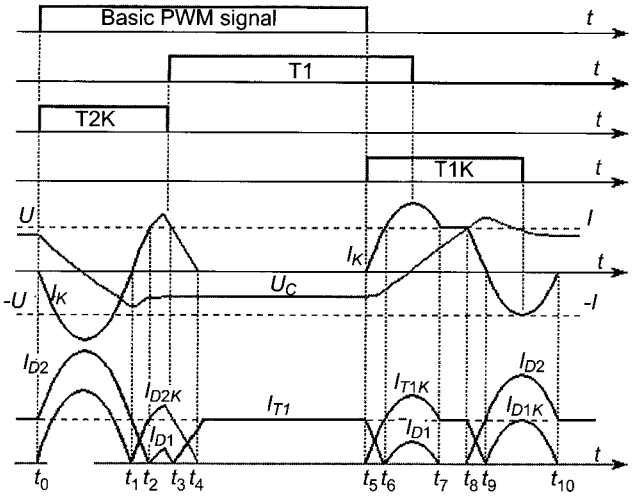

Fig. 2. The operational waveforms, $I > 0$

where:

I_K — current in resonant leg LC,
IT1 — T1 main switch current and corresponding symbols for the switches: T1K, T2K,
I_{D1} — D1 diode current and corresponding symbols for the diodes: D1K, D2, D2K
U — supply voltage,
U_C — capacitor voltage.

For the load current I<0, the control signals T2K and T1K have to be changed by place. Detailed operational principles of the six-switch ZCT inverter were explained in [2]. The control signals for the transistors are generated from the base PWM waveform. Additionally the actual sign of the phase inverter current must be determined. In a wide range of the load current, both turn-on and turn-off transitions for the main switch — T1 and T1K, T2K — auxiliary switches are processed at the zero-current condition. State plane trajectories of the six-switch ZCT inverter are plotted in Fig. 3.

2. SELECTION OF THE RESONANT TANK ELEMENTS

Design procedure for the resonant tank elements LC is the same as for the classic McMurray inverter. Values of the L, C elements are calculated by minimisation of the energy accumulated in the resonant tank [3]. The are following design variables: t_{00} — time available to turn-off the main switch, I_m — maximum value of the current in resonant branch that can turn-off main switch in the ZCT conditions. L and C are calculated as:

$$L = 0.397 \frac{U_C t_{00}}{I_m} \tag{2.1}$$

$$C = 0.893 \frac{I_m t_{00}}{U_C} \tag{2.2}$$

The variable X defined as $X = \frac{I_m}{I}$, is equal to optimal value 1,5 [3]. The resonant time period is defined as

$$T_0 = 2\pi\sqrt{LC} \tag{2.3}$$

Combining (2.1), (2.2) and (2.3), time may be given by

$$t_{00} = \frac{\pi\sqrt{LC}}{1.8} = \frac{T_0}{3.6} \tag{2.4}$$

3. INVERTER CONTROL TIMINGS

The control sign als within one switching cycle in one leg of the inverter, when load current I>0 are shown in Fig. 4.

Symbol t_d denotes the dead-time. The formula for the time t_{1on} was defined in [2].

$$t_{1on} = \frac{11T_0}{18} + t_{rr} \tag{2.5}$$

where t_{rr} is the reverse recovery time for the diodes: D1÷D6. In practice the time calculated from (2.5) has to be slightly longer to avoid branch short-circuit (between T1 and D2). From Fig. 2 it can be found, that the delay time t_{1off} is given as

$$t_{1off} = \frac{1}{4} T_o \tag{2.6}$$

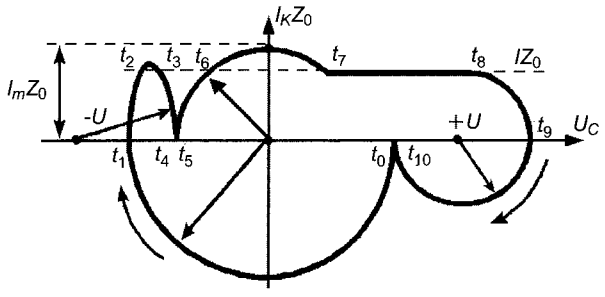

Fig. 3. State plane trajectories of the six-switch ZCT inverter

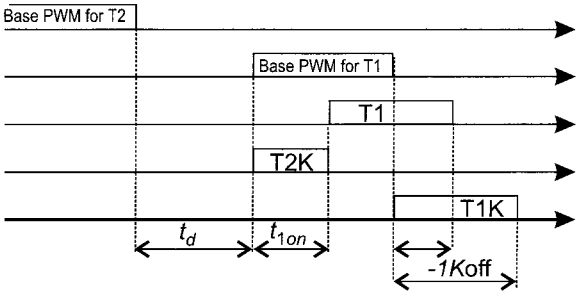

Fig. 4. The control signals, $I > 0$

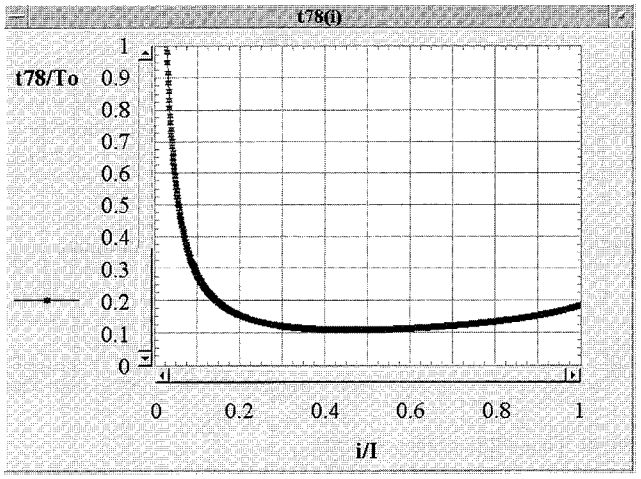

Fig. 5. Normalised time $\frac{t_{87}}{T_0}$ as a function of the load current $\frac{i}{I}$

Time t_{1Koff} is derived as

$$t_{1Koff} = \frac{T_0}{2} + t_{87} + \frac{T_0}{4} \tag{2.7}$$

The formula for the timing delay was derived in [2] and is given as

$$t_{87} = \frac{U - U_0 A \cos \arcsin\left(\frac{1}{XA}\right)}{I} C \tag{2.8}$$

where: $A = \cos \arcsin\left(\frac{1}{X}\right)$

Voltage U_0 is the initial voltage of the capacitor C at time t_0. During the time interval from t_7 to t_8, the capacitor C is being charged by a constant load current. In Fig. 8 the normalised time $\frac{t_{87}}{T_0}$ as a function of the normalised load current $\frac{i}{I}$ is shown.

4. DESIGN EXAMPLE

This chapter provides the design procedure for the 9kW six –switch ZCT inverter. In this example the intelligent power module – PM30RSF060 was selected to construct main switches. Maximum load current of the inverter is equal to 30A and the supply voltage U=300V. The design procedure is split in to following items:

A) In the electrical characteristics of this module the time available to turn-off the main switch — $t_{00} = 2.8\mu$s can be found.

B) Values of the L, C elements are calculated from (2.1) and (2.2). When the variable X = 1,5 then I_m = 45A. In practice the quality factor of the resonant branch $Q = \frac{1}{R}\sqrt{\frac{L}{C}}$ is equal or above 10, therefore the voltage $U_C = 0.9$U [2]. Following results were obtained: L = 6.67μH, C = 0.42μF. Resonant inductor should be built from a high frequency coil with a distributed air-gap and maximum magnetic flux density about 1T. This is indispensable to avoid saturation with a high peak of the resonant current. Low loss film-foil polypropylene capacitor should be used as a resonant capacitor. The resonant time period calculated from (2.4) is T_0=10.08μs.

C) From (2.5), (2.6) and (2.7) delay times: t_{1on} = 6.2μs, t_{1off} = 2.5 μs, t_{1Koff} = 10.5 μs were found.

It must be noticed that the times calculated above are a sum of the delay time generated by the control unit and build-in devices (photocouplers, transistors) delay times. Usually an experimental correction of the delay times is needed.

5. SIMULATION RESULTS

The proposed ZCT inverter top ology was simulated to verify the soft switching operation. Waveforms for one phase of the inverter were drawn. Figure 6 shows the turn-on and Figure 7 the turn-off transition of the main switch T1 at the positive constant (during switching cycle) load current i = 10A.

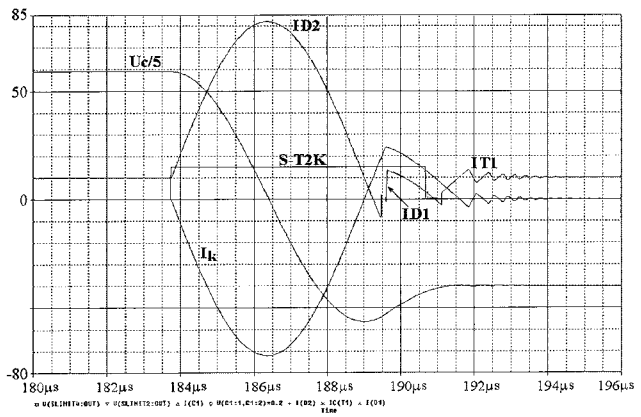

Fig. 6. Turn-on transition, i = 10A

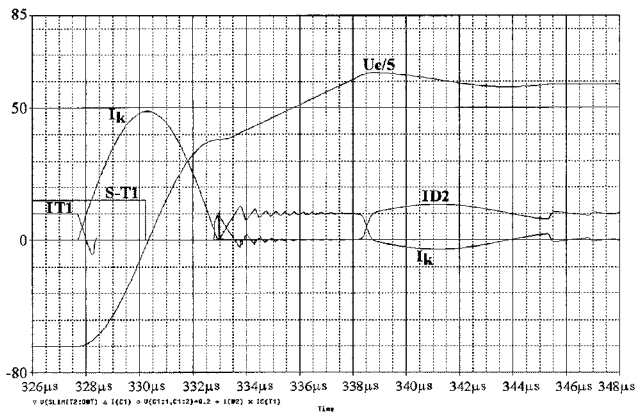

Fig. 7. Turn-off transition, i = 10A

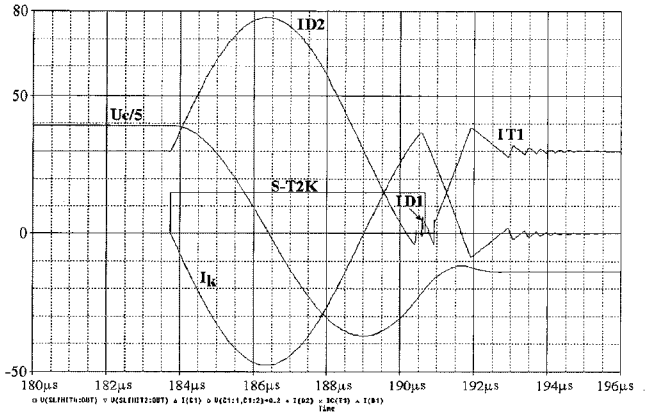

Fig. 8. Turn-on transition, I = 30A

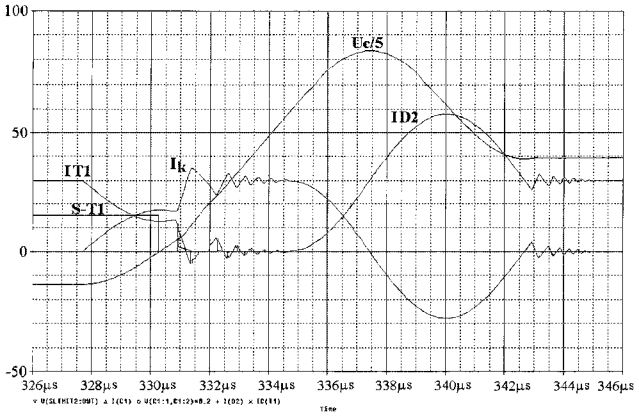

Fig. 9. Turn-off transition, I = 30A

S-T2K is the control signal at the gate of the T2K transistor. Similarly in Fig. 7, signal S-T1 control the gate of the T1 transistor. Analogous waveforms were simulated for maximum load current I = 30A at the turn-on transition — Fig. 8 and the turn-off transition — Fig. 9.

Comparing the plots in Fig. 6 and Fig. 8 with the draws in Fig 2, it can be seen that the T1 transistor is turned-on under zero current condition. At the same time when the signal S-T2K falls down the gate of the T1 transistor is driven high (see control waveforms in Fig.4). Turn-on of the T1 transistor begins when the parallel diode D1 stops to conduct and the ZCT condition is satisfied. The amplitude of the current I_K in the resonant branch depends directly on the initial voltage on the capacitor C. Referring to the waveforms shown in Fig. 2, at the time t_2 the resonant reloading of the capacitor C is stopped (diodes D1 and D2K conduct). If the load current i grows, then the capacitor voltage $U_{C(t2)}$ decreases. The voltage $U_{C(t2)}$ is equal to the voltage $U_{C(t5)}$ at the beginning of the turn- of process. Therefore in Fig. 9, for the maximum load current $i = I$, full soft switching turn-off transition of the T1 transistor is not achieved. Voltage $U_{C(t2)}$ is given as [2]

$$U_C(t_2) = -U_0 \cos \arcsin\left(\frac{i}{I_m}\right) \qquad (2.9)$$

Figure 10 illustrates the normalised voltage $\frac{U_C(t_2)}{U_0}$ as a function of the normalised load current $\frac{i}{I}$.

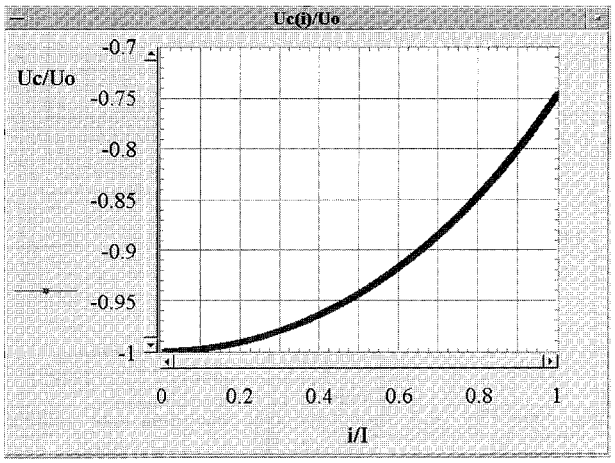

Fig. 10. The Voltage $\frac{U_C(t_2)}{U_0}$ as function of load current $\frac{i}{I}$

6. IMPLEMENTATION OF THE CONTROL ALGORITHM INTO CPLD DEVICE

To realise the control algorithm at least 6 counters are needed. Counters have to generate precise delay times. An additional logic produces signals for main and auxiliary switches. New generation of CPLD devices can be implemented to meet these requirements. CPLD devices consist of multiple copies of basic programmable logic elements. Logic elements can be interconnected to perform complex operations. Control functions are realised by MAX EPM7128 device from Altera. VHDL language or graphics editor may be used for description of the control algorithm. To shown principles of operations, graphics editor as description tool was chosen and compiled by Quartus II software. The main functional blocks of the control unit are shown in Figure 11.

Structure of the control blocks for each phase is similar and further only one block called Faza_A will be described. There are following input signals: CLK — clock, PWM_1, PWM_2 — basic PWM signals, I_A — sign of the phase

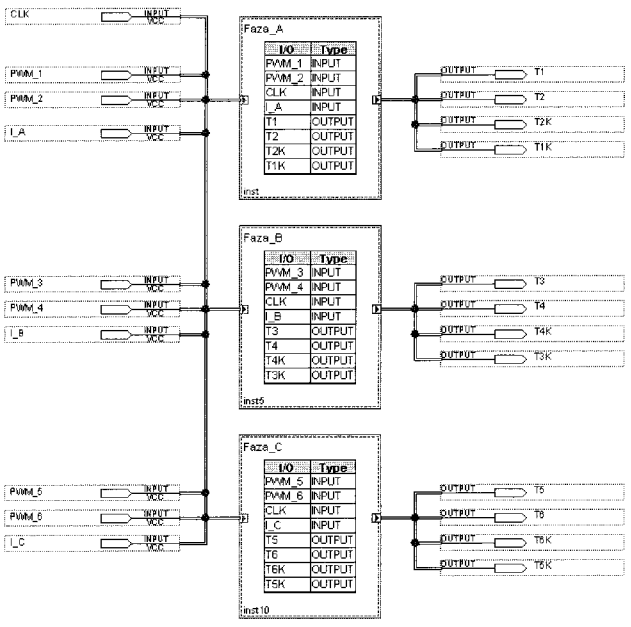

Fig. 11. Main functional blocs of the control unit

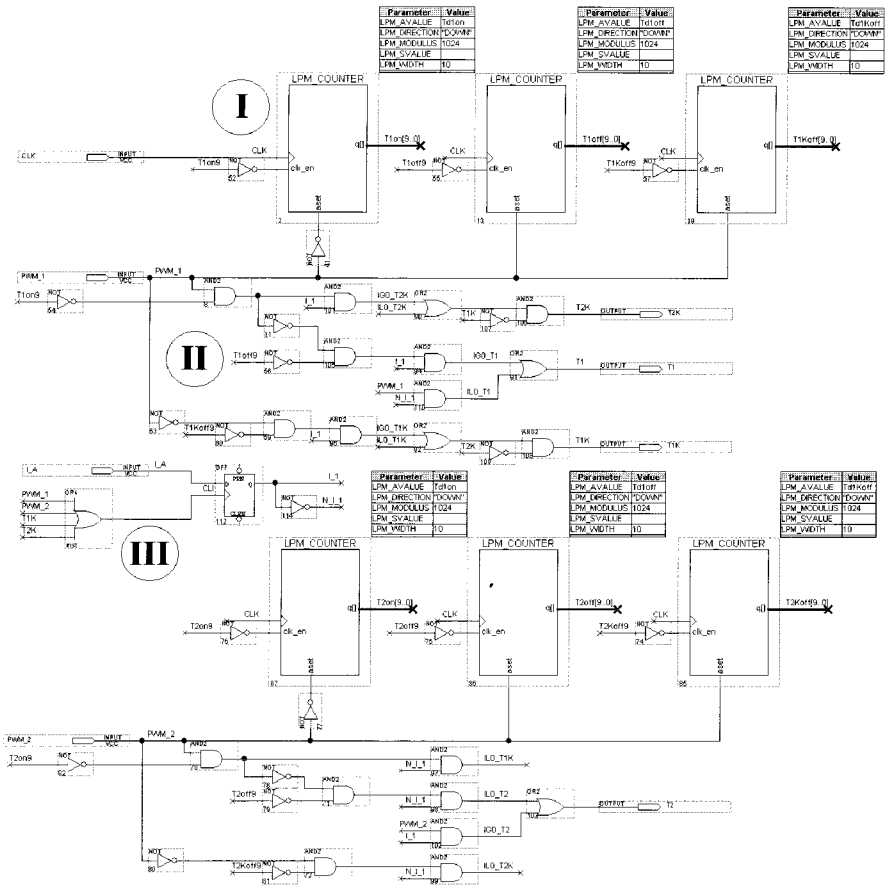

Fig. 12. Control logic

current. Internal block logic generates signals driving transistors: T1, T2, T2K, T1K. Details of the block Faza_A logic are shown in Figure 12.

Three counters in Figure 12 (signed as **I**) generate delay times: t_{1on}, t_{1off}, t_{1Koff} for positive phase load current $I > 0$. Several logic gates **II**, generate control signals for the transistors. Signal I_A (current sign) is synchronised by the D-type flip-flop **III**. Changes are possible only during the dead-time interval. For the load current $I < 0$ separate three counters are implemented to generate delay times. The results of time analysis are shown in Figure 13 and Figure 14.

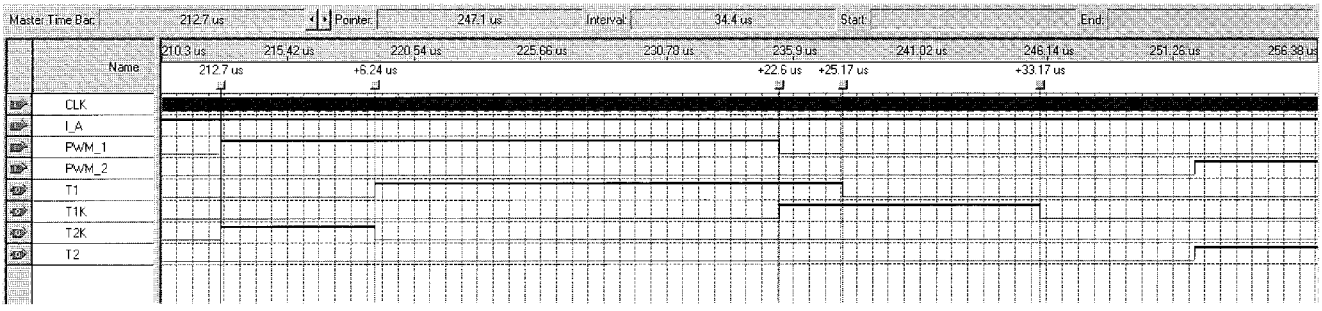

Fig. 13. Control timings, $I > 0$

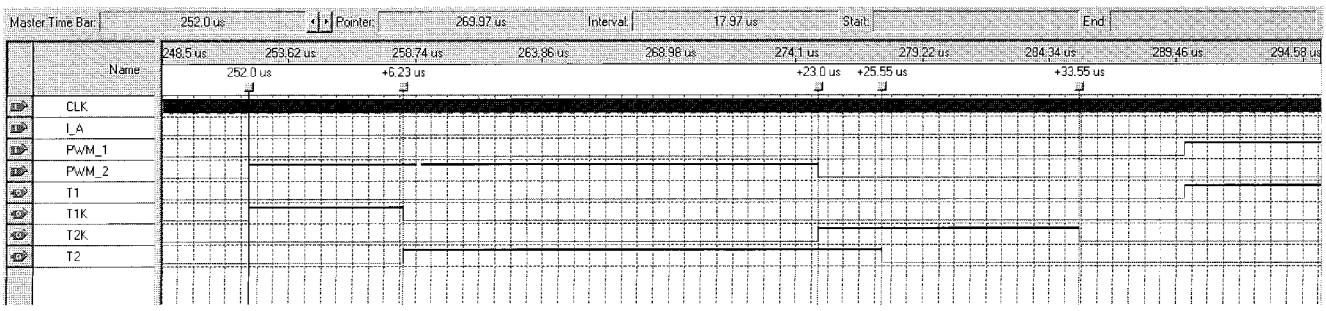

Fig. 14. Control timings, $I < 0$

7. CONCLUSIONS

The complete control system for six –switch ZCT inverter based on CPLD devices was presented. Derived mathematical equations were verified through simulation result. Soft switching transitions for the main switches at turn-on and turn-off in a wide range of the load current were obtained. Design procedure for high power ZCT inverter was shown. Requirements for the resonant tank elements L, C were formulated. Proposed control system needs only one chip device. Generated control waveforms are countered very precisely. Error depends on the clock frequency and can be less then 40ns. Control algorithm of the ZCT inverter slightly reduces width of the basic PWM waveforms produced by a master control unit. Instead of this the ZCT inverter topology offers very good efficiency and should be used at high power applications. Described solution based on CPLD device offers significant reduction of cost and complexity.

8. REFERENCES

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