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OVERVIEW OF CLASS E INVERTERS

Przegląd falowników klasy E

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Summary: **A low-order Class E inverter family is the subject of consideration. The paper contains: the general definition of Class E switching conditions, the systematic classification of Class E inverter family members (e.g. into inverters with zero-voltage-switching and zero-current-switching, symmetric and asymmetric configuration, sinusoidal and nonsinusoidal output current), schematic diagrams of representative Class E inverters, their principle of operation and selected characteristics, and finally, the comparison of their main features and parameters.**

Streszczenie: **W pracy dokonano przeglądu i porównania falowników klasy E niskiego rzędu. W szczególności praca zawiera: ogólną definicję warunków przełączania w klasie E, systematyczną klasyfikację falowników klasy E (np. ze względu na przełączanie w zerze napięcia i zerze prądu, symetryczną i niesymetryczną konfigurację, sinusoidalny oraz niesinusoidalny prąd wyjściowy), schematy zastępcze reprezentatywnych falowników klasy E, opis ich zasady działania i wybranych właściwości oraz zbiorcze porównanie najważniejszych parametrów charakteryzujących ich właściwości.**

Keywords: high-frequency, resonant inverter, Class E and DE inverters, soft switching
Słowa kluczowe: wysoka częstotliwość, falownik rezonansowy, falowniki klasy E i DE, miękkie przełączanie

1. INTRODUCTION

Since the invention of the idea of Class E operation in seventies by Gruzdev, 1969, [1] (mentioned in [5]) and the Sokals, 1975, [12], many papers have been published in this area. They mainly take into account individual Class E inverters and do not present more general view of a Class E family. Only a few of them try to systematise the issue, e.g. [5, 11], but they only consider selected topologies and their basic features. The paper is aimed at giving a systematic overview and comparison of Class E inverter family members.

As the popularity of many high-frequency applications continues to grow, designers are forced to construct highly efficient (in the range of 90%), high-frequency (higher than 1 MHz) power inverters. Class E inverters meet these requirements (e.g. 1 kW, 13,56 MHz, 89%, [9]). Their additional numerous advantages, such as high density of power processing, high reliability, simplicity, low cost and size, cause they are often used in industrial, scientific and medical applications. For example, they are applied in induction and dielectric heating, plasma generation, laser power supplies, glass and lens coating, transmitters for communication, portable light sources, DC/DC converters and implanted systems for power supplying.

2. DEFINITION OF THE TERM "CLASS E"

Before entering the proper discussion of the subject, the following notions have to be clarified: ZVS, ZCS, Class E, and operation modes.

One technique that improves converter performance is soft switching. It is based on constraints imposed on the switching process of power devices (e.g. transistors). The process is characterised by means of the voltage across the device or/and the current through it. It is realised as *ZVS* (zero-voltage-switching), or/and *ZCS* (zero-current-switching), respectively. This greatly decreases the switching losses and simultaneously allows to get higher operating

frequencies and lower levels of electromagnetic interference (EMI).

The ideal solution is to have ZVS and ZCS conditions for both switch transitions, on and off. Molnar, [10], has proved that it is impossible. There is no configuration of linear circuit elements ensuring simultaneous ZVS and ZCS for both transitions, when nonzero output power is needed. At least a single jump of current or voltage must be tolerated. For example, a switch can be turned on at ZVS and ZCS simultaneously, and turned off at ZVS. It means that the jump occurs in the current waveform when the switch turns off — figure 3. In general, the last illustrates the *maximum soft switching* that takes place when the *Class E switching conditions* are fulfilled.

Class E is the set of converters that allow for the maximum soft switching. In this case a converter realises *optimum operation mode*. Besides, the two operation modes of a Class E converter are possible, *suboptimum* and *nonoptimum*. The first mode takes place when two jumps of current or voltage occur during the switch transitions. The second one, the nonoptimum operation mode, relates to three jumps. The term of *Class E* refers to resonant rectifiers, inverters, frequency multipliers, amplifiers and generators.

The presented above definition of a Class E converter is more general than that one presented by the Sokals [12] or Raab [11]. They only define a specific Class E converter by giving the three following objectives: the switch voltage should be delayed until the switch is off, the switch voltage should return to zero before turn-on and the slope of the switch voltage should be zero at turn-on.

The general definition of a Class E converter allows to construct a variety of circuit topologies containing a source, a switch and a load network which consists of resonant elements and a load. In order to ensure the optimum operation mode, the proper values of the elements and the control (duty ratio, switching frequency) should be chosen [3].

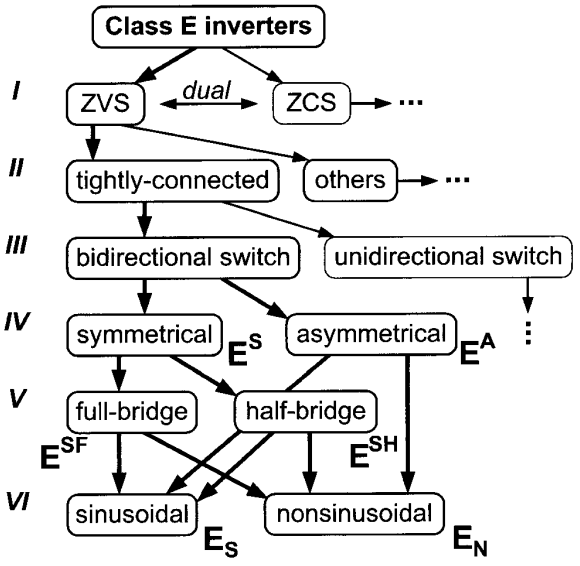

Fig. 1. Classification of low-order Class E inverter family

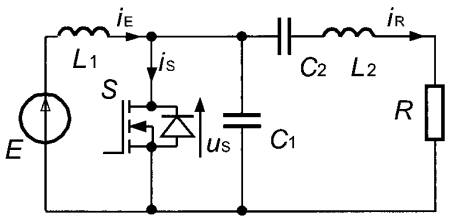

Fig. 2. Class E_S^A inverter

3. CLASSIFICATION OF CLASS E INVERTERS

The presented here inverters are members of a low-order Class E family. They include neither additional resonant circuits [7] nor matching circuits and transformers. Higher-order ones require more resonant components to achieve better transistor utilisation and are beyond the scope of the paper.

A Class E inverter family belongs to resonant converters and is depicted as a tree diagram in figure 1. There are the six consecutive levels of its division distinguished.

At the first level it is classified into ZVS and ZCS inverters. In the ZVS subfamily, ZVS conditions are preserved during both switch transitions (additionally ZCS is possible). The ZCS members are dual equivalents of the ZVS ones (e.g. their voltage and current waveforms are interchanged). In general, the ZVS are preferably over the ZCS at high switching frequencies because of eliminating switching losses and reducing parasitic oscillations caused by internal switch capacitance. The classification of the ZCS subfamily can be continued analogously to the ZVS ones taking into consideration the duality.

All members of the ZVS subfamily contain an external capacitor or capacitors connected in parallel with a switch [11]. This connection should decrease unwanted inductances of the switch-capacitor loop as far as possible, resulting in limiting parasitic oscillations and improving high-frequency operation.The special case of ZVS inverters is *tightly-connected* one that has only one parallel capacitor—figure 2. This capacitor is reduced to the internal capacitance of the switch at the highest operating frequency. In *others* the loop consists of the switch capacitance and two capacitors connected in series. They can be further classified in a manner analogous to that depicted in the tightly-connected inverters—figure 1.

The third level distinguishes two types of inverter switch. A *bidirectional switch* is composed of a switch and an antiparallel diode. The switch current can flow through it in both directions. The second type, a *unidirectional switch*, consists of a switch and a series diode and its current can flow in only one direction. The benefit of including either the antiparallel diode or the series diode in the switch is that the inverter can operate in optimum or suboptimum mode for bounded variations in load, operating frequency, and switch duty ratio [6]. The parallel diode, for example, accelerates the time at which the switch turns on. Since the switch turns on at zero voltage, the turn-on switching losses are zero, yielding high efficiency. In the case of the bidirectional switch, the lower values of parasitic inductances can be obtained. The disadvantage of the unidirectional switch is associated with

Table 1. Comparison of different ZVS Class E inverters

	E_S^A	E_{N1}^A	E_{N2}^A	E_S^{SH}	E_{N1}^{SH}	E_{N2}^{SH}	DE_S^{SH}	DE_N^{SH}
x_{L1}	∞	∞	0.409	∞	∞	0.408	—	—
x_{L2}	10.000	1.789	0.000	10.000	1.217	0.000	10.000	0.568
x_{C1}	5.056	4.595	0.972	2.740	2.943	0.970	17.490	10.890
x_{C2}	8.790	0.000	0.000	8.839	0.000	0.000	9.559	0.000
r_{DC}	1.821	2.783	0.523	0.437	0.445	0.172	6.030	6.442
P_P	0.099	0.086	0.065	0.097	0.091	0.099	0.145	0.157
P_R	0.182	0.173	0.159	0.181	0.170	0.177	0.296	0.301
thd	0.044	0.295	0.521	0.012	0.079	0.221	0.022	0.183
f_m	1.000	1.735	1.500	0.879	0.881	1.093	0.242	0.422

where:

x_{L1}, x_{L2}, x_{C1}, x_{C2} — relative reactances of L_1, L_2, C_1, C_2 (e.g. $x_{L1}=2\pi f L_1/R$),

$r_{DC} = R_{DC}/R$ — relative resistance presented to dc-power supply,

P_P — output power per switch for a peak switch voltage of 1 V and a peak current of 1 A,

P_R — output power per switch for a peak voltage of 1 V and a RMS switch current of 1 A,

$thd = (\sum_{i=2}^{\infty} I_{Ri}^2)^{1/2} / I_{R1}$ — total harmonic distortion of output current,

$f_m = f_m/f_{mESA}$ — relative maximum operating frequency of inverter.

the internal capacitance. This capacitance is charged via the series diode to the peak value of the switch voltage and next, when the switch turns on, it is discharged. Hence, the power is dissipated in the switch and the efficiency is reduced. The classification of the unidirectional switch members can be carried out analogously to the bidirectional switch inverters.

Taking into account the symmetry of a Class E inverter topology, symmetrical and asymmetrical inverters are distinguished [11]. In the *symmetrical* ones even harmonics are suppressed at their load. They can be realised as *half-bridge* or *full-bridge* configurations containing two or four switches, respectively. The *asymmetrical* Class E topologies employ a single switch. They do not cancel any harmonics but are easier to construct and control.

Finally, the last level classifies Class E inverter members according to the shape of load current. They are divided into the inverters with *sinusoidal* and *nonsinusoidal* load current [4, 11].

For clarity some symbols are proposed (fig. 1) where E stands for Class E. Superscripts S, A, F, H mean symmetrical, asymmetrical, full- and half-bridge, respectively. Subscripts S and N represent sinusoidal and nonsinusoidal output current.

4. SELECTED CLASS E INVERTER MEMBERS

Selected ZVS Class E inverters that are representative of a Class E family are described in this section. All of them are members of a tightly-connected subfamily with a bidirectional switch. Their mutual correlation is discussed.

MOSFET transistors usually find practical applications in high-frequency Class E inverters as switches. Because of this, their symbol is used in the presented schematic diagrams. Moreover, in the range of a few MHz their inherent diodes can be applied as an antiparallel diode [3], and in this case the switch construction is very easy.

All further explanations and needed calculations of inverter parameters are made assuming that a transistor with a diode operate as an ideal switch (i.e. have zero resistance when on, infinite resistance when off, no associated parasitic capacitances or inductances, and zero transition times), passive components are ideal (linear, their self-resonant frequencies are much higher than operating frequency and, except R, lossless). All waveforms shown bellow have been computed for the supply voltage source $E = 1$ V and the load $R = 1\ \Omega$. The rest of inverter parameters can be obtained using table 1.

4.1. Class E_S^A and E_N^A inverters

The asymmetrical, sinusoidal Class E_S^A inverter is depicted in figure 2. It consists of a switch S driven at a frequency f and a turn-on duty ratio D (usually $D = 0.5$), an inductor L_1, a passive load network (C_1, C_2, L_2) whose self-resonant frequencies are slightly different than the operating frequency, by which the energy from power supply is transmitted to the load R. In most cases the inductor L_1 ensures a constant input current ($di_E/dt = 0$) but the case $di_E/dt \neq 0$ is also applicable [13].

The inverter operation can be discussed based on fig. 2 and 3. The transistor is turned on and off periodically. When the switch S is open, the difference between the input current i_E and the output current i_R flows into the capacitor C_1. When the switch S is closed, the current difference flows through it. In order to ensure the maximum soft switching (ZVS-on, ZCS-on, ZVS-off), the switch voltage u_S and its derivative du_S/dt must be zero at turn-on. It is made by the proper choice of the values of C_1, C_2 for given L_2, R, f, D.

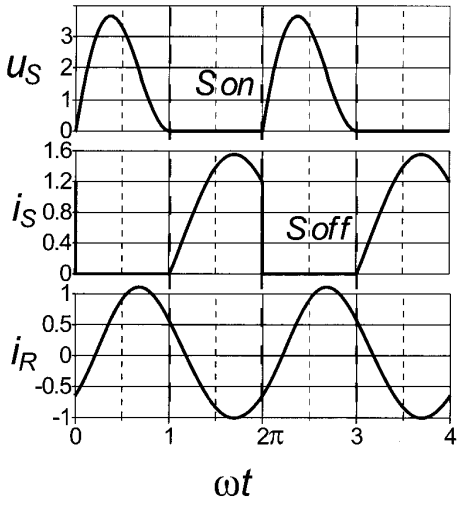

Fig. 3. Waveforms of Class $E_S{}^A$ inverter from fig. 2

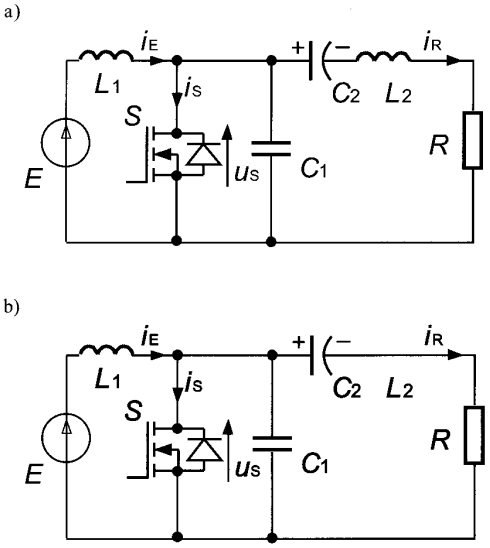

Fig. 4. Class E inverters: (a) $E_{N1}{}^A$, (b) $E_{N2}{}^A$

Simultaneous computations of the capacitances C_1 and C_2, ensuring the maximum soft switching conditions for given R, f, D, and a reduction in the value of L_2 lead to increasing the capacitance C_2. Finally, for the loaded quality factor $Q = 1.789$ (defined as $2\pi f L_2 / R$), the capacitor C_2 is a blocking capacitor—figure 4a. The relevant waveforms of the $E_{N1}{}^A$ inverter are shown in figure 5a. The switch current i_S is exponential and the load current i_R is nonsinusoidal.

Continuing this, when the inductance L_1 is decreased and the values of C_1, L_2 are computed for the $E_{N1}{}^A$ inverter, the inductance L_2 reduces, and in the end, approaches zero—figure 4b. The $E_{N2}{}^A$ inverter is a next member of Class E nonsinusoidal inverters. Its switch current i_S builds up linearly—figure 5b.

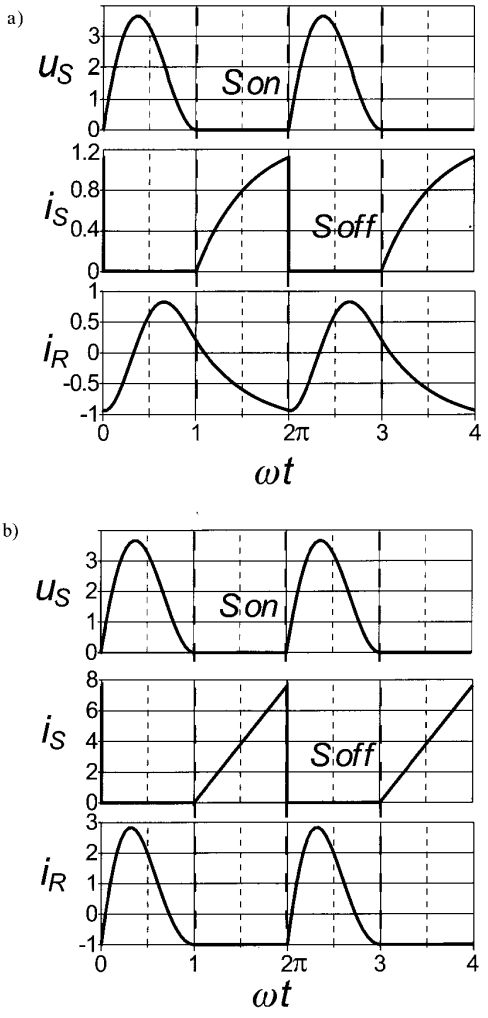

Fig. 5. Waveforms of Class E inverters: (a) $E_{N1}{}^A$, (b) $E_{N2}{}^A$

4.2. Class $E_S{}^S$ and $E_N{}^S$ inverters

A symmetrical configuration offers a means of combining more switches to obtain larger output power, and at the same time, it provides the suppression of load even harmonics. Figure 6 depicts such inverters. The transistors are driven alternatively (in $E_S{}^{SF}$ in pairs, S_1–S_4 and S_2–S_3). The switch voltage u_S and current i_S waveforms are very similar to those obtained in the $E_S{}^A$ inverter (fig. 3) and the differences are caused by the form of the load current and the average values of the switch voltage and current. Assuming the same values of R, L_2, f, the Class $E_S{}^{SH}$ inverter in comparison with the $E_S{}^A$ one needs the same capacitance C_2 and nearly twice the capacitance C_1—table 1. Considering the $E_S{}^A$ and $E_S{}^{SF}$ inverters, they have almost the same values of C_1 and C_2.

The Class $E_S{}^{SH}$ and $E_S{}^{SF}$ inverters can be transformed in their nonsinusoidal equivalents in a manner analogous to that described in the case of the $E_S{}^A$. It is illustrated by the example of the $E_S{}^{SH}$ inverter. When the loaded quality factor Q decreases, the capacitance C_2 increases and, for $Q = 1.217$, approaches infinity. The relevant waveforms are shown in

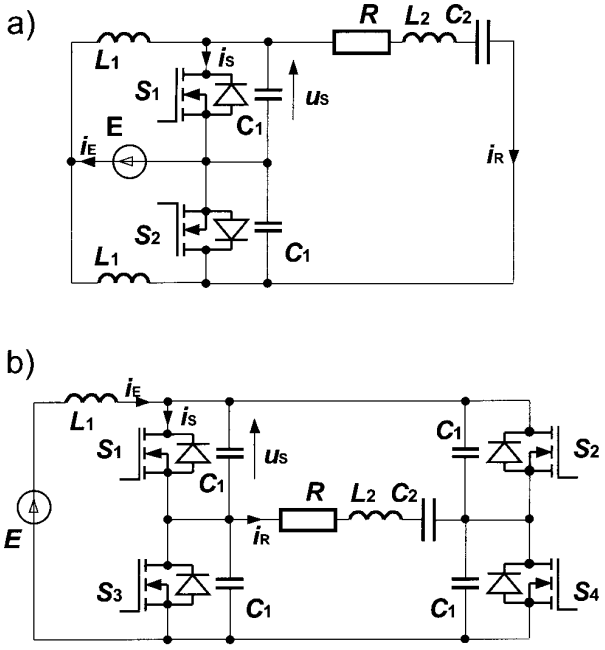

Fig. 6. Class E inverters: (a) E_S^{SH}, (b) E_S^{SF}

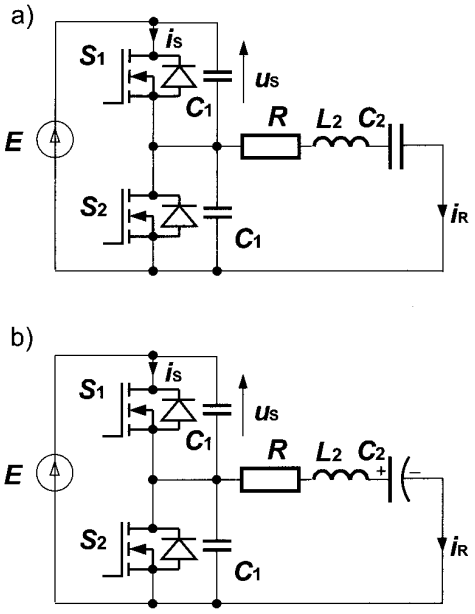

Fig. 8. Class DE inverters: (a) DE_S^{SH}, (b) DE_N^{SH}

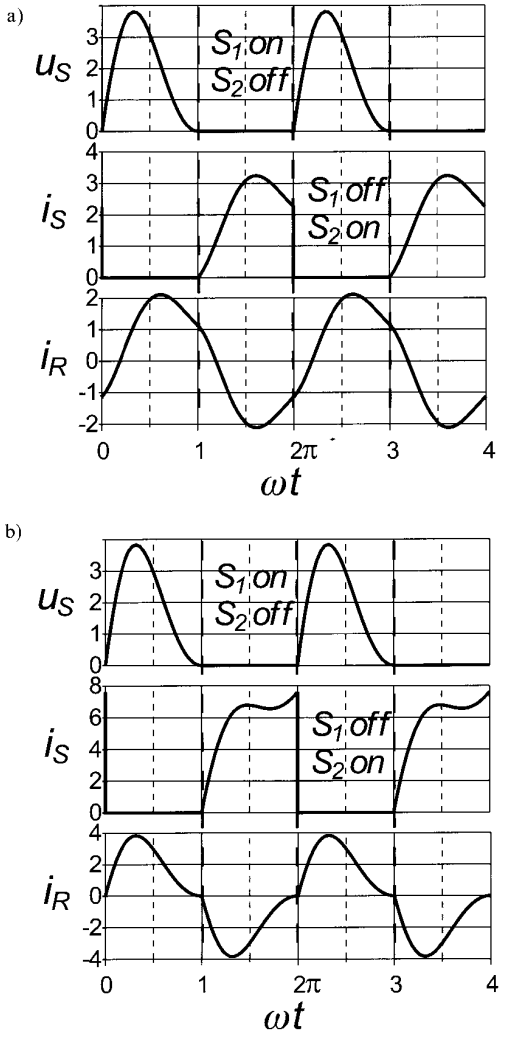

Fig. 7. Waveforms of Class E inverters: (a) E_{N1}^{SH}, (b) E_{N2}^{SH}

figure 7a. Next, a reduction in the inductance L_1 leads to decreasing the value of L_2, which finally, reaches zero. The voltage and current waveforms for the E_{N2}^{SH} inverter are depicted in figure 7.b. In both E_{N1}^{SH} and E_{N2}^{SH} inverters the current waveforms are different in shape from those computed for the asymmetrical ones.

4.3. Class DE_S^S and DE_N^S inverters

A Class DE inverter is a hybrid of Class D and E inverters. The maximum soft switching conditions are fulfilled (Class E) and simultaneously a peak switch voltage during turn-off is limited to the dc-input voltage E (Class D). Class DE, like Class E, is preferable to Class D at frequencies higher than 1 MHz because it is more efficient. The idea of Class DE operation has been introduced by El-Hamamsy [2] and Koizumi [8].

The Class DE_S^{SH} inverter, figure 8a, consists of a series-resonant circuit, a load resistance, and two bidirectional switches with shunt capacitors, which can absorb parasitic capacitances of the switches. The transistors S_1, S_2 are driven on and off with the dead time in opposite phase. For the case shown in figure 9a the duty ratio D equals 0.4. During the dead time, the sinusoidal output current i_R charges one shunt capacitor and discharges the other, and as a result the capacitor voltages are E and zero, respectively.

Full-bridge configurations of Class DE inverters are also possible. They need four switches and twice the value of the shunt capacitors C_1.

The sinusoidal DE_S^{SH} inverter has its nonsinusoidal equivalent—figure 8b. The DE_N^{SH} inverter in comparison with the DE_S^{SH} one requires a lower value of the loaded quality factor Q, e.g. $Q = 0.568$ for $D = 0{,}4$. The capacitor C_2 blocks the dc-voltage of $E/2$. The waveforms for this case are shown in figure 9b.

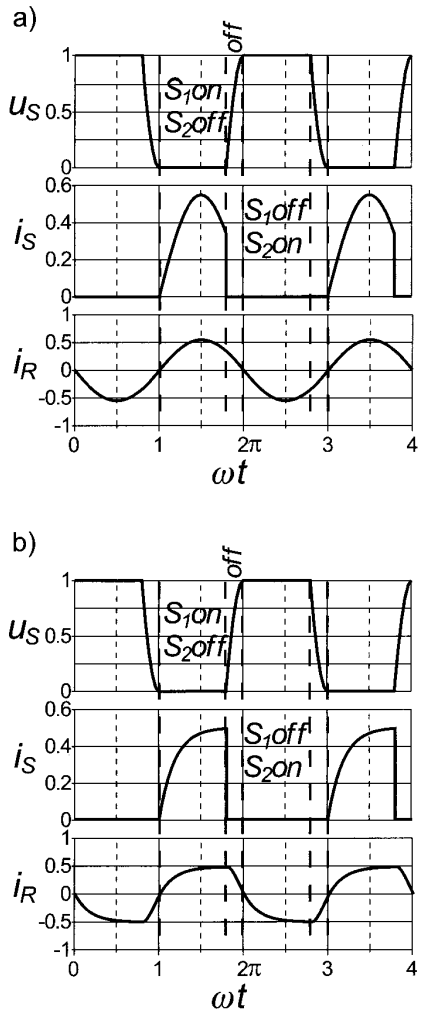

Fig. 9. Waveforms of Class DE inverters: (a) DE_S^{SH}, (b) DE_N^{SH}

5. COMPARISON OF ZVS CLASS E INVERTERS

Table 1 contains selected data computed for the Class E inverters discussed here. The table includes values of circuit elements and a few more general parameters, which characterised features of the inverters. They have been calculated for duty ratio $D = 0.4$ in the case of Class DE inverters and $D = 0.5$ for others.

Relative input resistance r_{DC} is higher for the E^A inverters in comparison with the E^{SH} ones, and even higher for the DE^{SH}.

Powers P_P and P_R reflect transistor utilisation and their values provide a means of comparing different types of inverters. They have almost the same values for sinusoidal and nonsinusoidal Class E inverters and are higher for Class DE inverters ($P_{P,R(DE)}/P_{P,R(E)} = 1.5$). This is because the beneficial shape of switch voltage waveforms of the last case, which is nearly rectangular.

For nonsinusoidal inverters values of *thd* are high and for sinusoidal ones are low, particularly for symmetrical configurations, which is obvious.

Maximum operating frequency f_m has been computed for the following assumptions: in all inverters are used the same transistors, the capacitance C_1 is only made up by the output transistor capacitance, and the transistors have the identical voltage and current stresses. The E_N^A inverters have higher frequency limit, the E^S similar and the DE much lower in comparison with obtained in the E_S^A inverter.

6. CONCLUSIONS

The general definition of Class E, the classification in the form of a tree diagram of Class E inverter family, the most important features and the comparison of ZVS Class E family members have been presented in the paper.

In ZVS Class E inverters their switch voltage and current waveforms satisfy the Class E switching conditions. Because parasitic capacitance of a switch can be included in capacitance of a resonant circuit and power dissipated during each transistor switching is minimised, they are applied in high-frequency range.

Symmetrical and asymmetrical configurations of Class E inverters are possible. The symmetrical ones employ at least two transistors and provide even harmonics cancellation.

Most highly efficient, high-frequency power inverters are members of Class D or Class E family. Frequency borderline between these families depends on power, voltage, and efficiency and lies in a few MHz range.

Class E inverters are easier to construct and control, have the highest possible frequency limit but their voltage and current waveforms are peaked. On the other hand, a Class DE family has better transistor utilisation but is more difficult to control (dead time) and its maximum frequency is considerably lower.

The future researches should enhance the presented here classification including omitted members of a Class E family, low- and high-order ones.

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