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VOLTAGE SOURCE POWER LINE CONDITIONERS

Napięciowe kondycjonery energii

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Summary: **The paper presents a different way for a power quality conditioning. The different way means parallel connection of the sinusoidal voltage source with the network, therefore it is possible to "isolate" load from source and vice versa. Described conditioner makes possible to get: i) sinusoidal source current; ii) reactive power compensation; iii) load voltage stabilization; iv) balanced source in conditions of the unbalanced load (in 3-phase networks). As a sinusoidal voltage source in 3-phase network, the four level cascade based Voltage Source Converter (VSC) has been used. The effectiveness of the Voltage Source Power Line Conditioners (VPLC) is carefully outlined, while the systems general performance and flexibility are intensively investigated. To confirm results of the theoretical analysis some experimental results were presented.**

Streszczenie: **W artykule opisano inny sposób poprawy jakości energii. Inny sposób oznacza tutaj równoległe połączenie z siecią źródła napięcia sinusoidalnego w wyniku czego możliwa jest „izolacja" obciążenia od sieci i *vice versa*. Opisany kondycjoner umożliwia uzyskanie: i) sinusoidalnego prądu sieci; ii) kompensacji mocy biernej; iii) stabilizacji napięcia na obciążeniu; iv) symetryzacji sieci w przypadku niesymetrycznego obciążenia (w sieciach 3-fazowych). Jako źródło napięcia sinusoidalnego, w sieciach 3-fazowych, wykorzystano kaskadowy czteropoziomowy falownik VSI. W artykule zbadano skuteczność Napięciowego Kondycjonera Energii (VPLC) oraz opisano jego podstawowe właściwości. Wyniki analizy teoretycznej zostały poparte wynikami badań eksperymentalnych.**

Keywords: power quality, active line conditioners, voltage source converter, multilevel converter, current harmonic compensation, reactive power compensation
Słowa kluczowe: jakość energii, aktywne kondycjonery, falownik napięcia, falownik wielopoziomowy, kompensacja harmonicznych prądu, kompensacja mocy biernej

1. INTRODUCTION

The goal of this paper is to present simple, VPLC systems and to investigate, which extent they are suited to fulfill a wide range of different tasks:
— to prevent "dirty" loads from polluting the electrical distribution network (current conditioning mode);
— to protect sensitive loads from line disturbances as voltage sags (voltage restoring mode).

The intention is to combine circuit simplicity with flexibility in performance.

In professional literature [1, 2, 6, 7] there are described many different ways how to "isolate" sources from disturbances introduced by the nonlinear loads and vice versa. For example to compensate higher harmonics of the current, produced by the nonlinear loads, Active Power Filters (APF) can be used [1, 2]. In those systems (independent with control algorithm) there is need to extract compensating components, from measured load or source currents (it depends if control algorithm is in open or closed loop), therefore the filtration quality is as good as it is possible to extract compensating components and shape them.

The paper presents a different way of a power quality improvement. In a presented solution there is no need to measure load or source currents, or to extract any compensating components, power quality improvement is possible using parallel connected VSC acts as a sinusoidal, with fundamental frequency, voltage source [3], therefore described conditioner makes possible to get:

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— sinusoidal source current;
— reactive power compensation;
— load voltage stabilization;
— balanced source in conditions of the unbalanced load (in 3-phase networks).

Because conditioner has to "produce" sinusoidal, with fundamental frequency, VSC are the perfect solution in this case. Onto needs of the Voltage Power Line Conditioners (VPLC) in 3-phase networks, the four-level cascade based voltage source inverter was developed [4, 5].

The paper consists of three major parts. First, Voltage Source Power Line Conditioner with special regard to current conditioning and the reactive power compensation mode in chapter 2 – will be explained. Chapter 3 presents 1-phase VPLC solutions. This chapter also includes enhanced controls algorithm and experimental results for 1-phase VPLC. The presentation of the major properties and experimental results of the four level cascade based VSC, in chapter 4 will be finally demonstrated.

2. VPLC – BASIC PROPERTIES

2.1. General property

Figure 1 shows a simplified scheme of the investigated VPLC and it's control algorithm. The major difference between this conditioner and the others lies in the way of source current harmonics compensation. The "classic" conditioner has to detect the load current harmonic and generate the compensating components [1, 2]. Presently investigated system does not need to detect the load current harmonics, because they are naturally absorbed by the VSC, which has the attribute to "isolate" the load from the source (power system) [3].

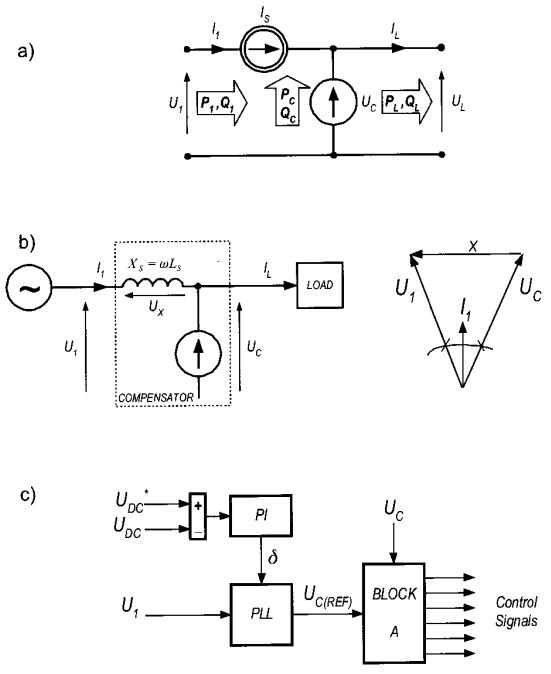

Fig. 1. Voltage source power line conditioner: a) model; b) one line diagram; b) simplified control algorithm

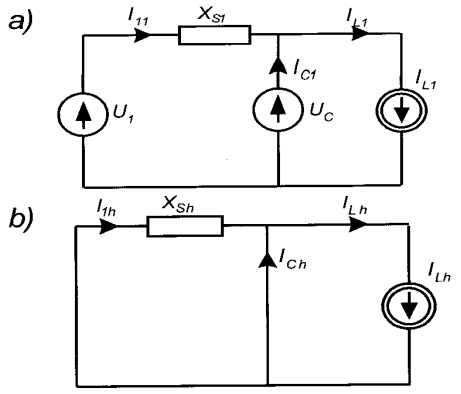

Fig. 2. VPLC equivalent circuits for: a) fundamental frequency; b) higher harmonics

In control algorithm PLL generates signal $U_{C(REF)}$ whose frequency is equal to that of the network and phase is shifted in relation to U_1 with angle d. Block A stabilizes voltage on the load at the reference value by means of a closed-loop control error between the RMS U_C and the reference voltage $U_{C(REF)}$. To keep total DC link voltage on constant value PI controller was implemented.

Described conditioner consists of two major elements: series reactance X_S (in first approximation represented by current source I_S=I_1) and controlled sinusoidal voltage source U_C, both inserted between the source and the load. In situation when voltage U_C, generated by the inverter, is shifted, in regard to the network voltage U_1, with angle d, there is possible power flow from source to load and source current I_1 becomes sinusoidal.

2.2. Harmonics suppression

The equivalent circuits of the VPLC at different conditions are presented in Figure 2. In those circuits X_{S1} represents series reactance for fundamental frequency; respectively X_{Sh} represents series reactance for higher harmonics. U_C and U_1 are respectively the fundamental part of the VSI output voltage and source voltage. Additionally I_{L1} represents fundamental part of the load current and I_{Lh} higher harmonics of the load current.

As we can see, from Figure 2b for higher harmonics, because source voltage is sinusoidal therefore VSI produces also shifted sinusoidal component with fundamental frequency, both voltage sources U_1 and U_C can be neglected and because X_{Sh}>>0, load current is given by:

$$I_{Lh} = I_{Ch} \tag{1}$$

Therefore, the compensation characteristics to load can be written as:

$$I_{1h}/I_{Lh} \Rightarrow 0 \qquad (2)$$

On the base of above we can tell that considered conditioner provides "perfect" compensation of the load current higher harmonics, the voltage U_C generated by the VSC has the effect of "isolating" source from the non-linear loads.

2.2. Reactive power compensation

Proposed arrangement (Fig. 1) makes also possible reactive power compensation. Let us determine equation on input power factor.

For defined voltages:

$$\vec{U}_1 = U_1\cos(\delta)+jU_1\sin(\delta) \qquad (3)$$

$$\vec{U}_L = \vec{U}_C = U_C \qquad (4)$$

where: $\delta \angle(\vec{U}_1,\vec{U}_C)$,

equations on active and reactive powers are as follows:

$$P_1 = \frac{U_1U_C}{X_S}\sin(\delta)\,; \quad Q_1 = \frac{U_1^2}{X_S} - \frac{U_1U_C}{X_S}\cos(\delta) \qquad (5)$$

$$P_C = P_L - \frac{U_CU_1}{X_S}\sin(\delta) \qquad (6)$$

$$Q_C = \frac{U_C^2}{X_S} - \frac{U_CU_1}{X_S}\cos(\delta) + Q_L \qquad (7)$$

where: P_L active and Q_L reactive power determined for U_L voltage and load parameters.

On the base of above equations, with assumption that $U_1=U_C$ and taking into account that in steady-state there is no active power exchange with VSI, i.e. $P_1=P_L$ and $P_C=0$, equation on input power factor is as follows:

$$PF_1 = \cos\left(0.5\arcsin\left(\frac{P_LX_S}{U_1^2}\right)\right) \qquad (8)$$

and active P_1 and reactive Q_1 power are equal:

$$P_1 = \frac{U_1^2}{X_S}\sin(\delta)\,; \quad Q_1 = Q_{1N} = \frac{U_1^2}{X_S}[1-\cos(\delta)] \qquad (9)$$

On the base of curves presented in Figure 3 there is possible to say that due to small values of inductance L_S the phase angle between voltages U_1 and U_C is very small and hence the phase angle between I_1 and U_1 is even smaller. As a result, the input power factor is near unity.

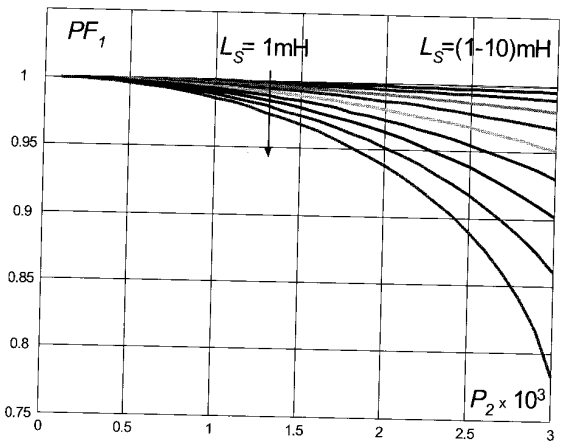

Fig. 3. Changes of the input power factor

For purpose of the reactive power compensation the magnitude U_C has to be controlled to be equal to that of U_1, because any differences between them are leading to considerable growth of the input reactive power, see Figure 4. The same amplitudes can be achieved by adjusting the converter modulation index.

If amplitude $U'_C \neq U_C=U_1$ and angle δ' is as follows:

$$U'_C = U_1\sqrt{1+\sin^2(\delta)}\,, \quad \delta' = \arcsin\left(\frac{\sin(\delta)}{\sqrt{1+\sin^2(\delta)}}\right) \qquad (10)$$

then

$$P_1 = \frac{U_1U'_C}{X_L}\sin(\delta') = \frac{U_1^2}{X_L}\sin(\delta) \qquad (11)$$

In this case

$$Q_1 = \frac{U_1^2}{X_1} - \frac{U_1U'_C}{X_1}\cos(\delta') = 0 \qquad (12)$$

3. VPLC — 1-PHASE SOLUTIONS

3.1. Parallel VPLC system

Investigated 1-phase VPLC system, presented in Figure 5, makes also possible to get sinusoidal source current I_1, input power factor near unity and, in situation of sinusoidal source voltage, load voltage without deformations. In this circuit, a two level PWM modulation VSC as U_C voltage source was used. Figure 6 presents the block diagram of the simplified control algorithm of the 1-phase VPLC (Fig.6).

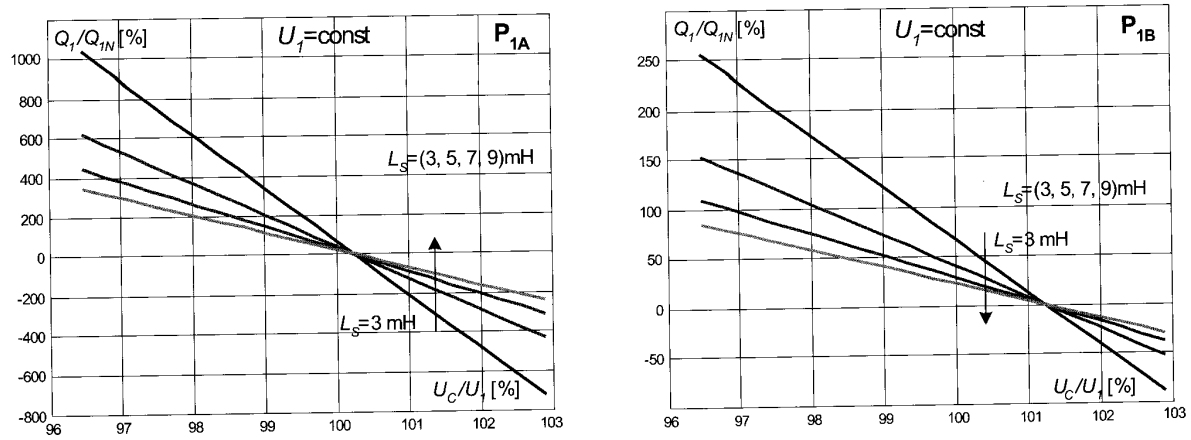

Fig. 4. Influence of the U_C on input reactive power, where: $P_{1A} < P_{1B}$, Q_{1N} – input reactive power when $U_1 = U_C$

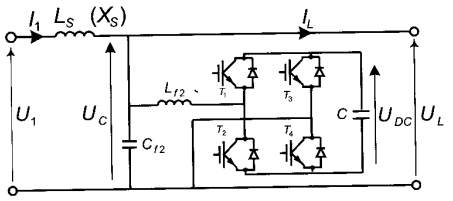

Fig. 5. Single-phase parallel VPLC circuit

If real power supplied by the system is greater than the load demand, the surplus portion will be absorbed by the VSC and thus cause the DC link capacitor voltage to increase. If real power supplied by the system is less than the load demand, the DC link capacitor voltage will decrease. To regulate the DC link capacitor voltage a PI controller was used. This controller uses the error between the reference $U_{DC(REF)}$ and the actual DC voltage U_{DC} as a feedback signal. The PI controller produces the phase angle d to control the real power absorbed or supplied by the VSC thus regulates the DC link capacitor voltage.

In steady state (neglecting the losses in the VSC) the angle d corresponds to the real power supplied by the network (the real power supplied by the network has to be equal to the real power of the load). In this case instantaneous power taken/delivered to the VSC arrangement does not contain constant as well as variable component and it changes in accordance with dependence:

$$p_C(t) = Q_C \sin(2\omega t + 2\delta) \tag{13}$$

From here the variable component of the energy accumulated in capacitor C, of the DC circuit, express equation:

$$\tilde{\Delta}E = \int p_C(t)\,dt = -\frac{Q_C}{2\omega}\cos(2\omega t + 2\delta) \tag{14}$$

On basis of dependence (14) as well as formula onto energy accumulated in capacitance in dependence on voltage we receive the following equation:

$$\left|\Delta E_{max}\right| = C \cdot \left(U^2_{DC(max)} - U^2_{DC(min)}\right)/2 = Q_C/\omega \tag{15}$$

where:

ΔE_{max} — peak-to-peak value of changes of energy in DC circuit;

$U_{DC(max)}$, $U_{DC(min)}$ — maximum and minimum value of voltage U_{DC}.

Taking into account that:

— reference voltage value

$$U_{DC(REF)} = \left(U_{DC(max)} + U_{DC(min)}\right)/2 \tag{16}$$

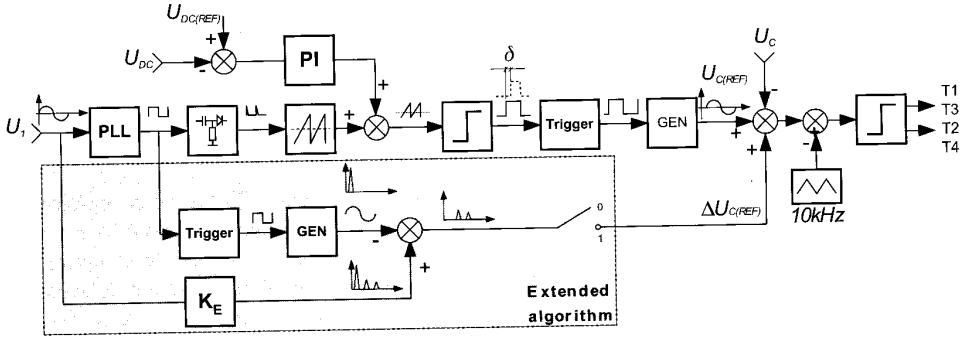

Fig. 6. Block diagram of the control algorithm of the 1-phaseVPLC system

— relative amplitude of pulsation of voltage U_{DC}

$$\varepsilon_{U_{DC}} = \Delta U_{DC} / U_{DC(REF)} \tag{17}$$

where:

$$\Delta U_{DC} = \left(U_{DC(max)} - U_{DC(min)}\right)/2 \tag{18}$$

equation (17) can be expressed as:

$$\left|\Delta E_{max}\right| = Q_C/\omega = 2 \cdot C \cdot \varepsilon_{U_{DC}} \cdot U^2_{DC(REF)} \tag{19}$$

With assumption, that VPLC system is loaded with linear load with $\cos(\varphi_L)$ power factor, taking into account dependences (6) and (7), as well as fact, that in steady state $P=P_1=P_L$, demand onto reactive power Q_C of the VSI arrangement can be calculated from dependency:

$$Q_C = P_{max}\left(1 + S - \sqrt{1-\gamma^2} + \gamma \cdot \mathrm{tg}(\varphi_L)\right) \tag{20}$$

where:

$$P_{max} = \frac{U_1 \cdot U_C}{X_S}, \quad S = \frac{U_C - U_1}{U_1}, \quad \gamma = \frac{P}{P_{max}}$$

In this of case, as it results from equations (19) and (20), DC circuit capacity can not be smaller as calculated on basis of inequality:

$$C \geq P_{max} \frac{\left(1 + S - \sqrt{1-\gamma^2} + \gamma \cdot \mathrm{tg}(\varphi_L)\right)}{2 \cdot \omega \cdot \varepsilon_{U_{DC}} \cdot U^2_{DC(REF)}} \tag{21}$$

where:

$$U_{DC(REF)} \geq \left[\sqrt{2} \cdot (1+S) \cdot U_1\right] / \left(1 - 2 \cdot \varepsilon_{U_{DC}}\right) \tag{22}$$

In special case, when $U_C=U_1$ (i.e. $S=0$) as well as relatively small load power (about $\gamma<0{,}2$), instead of formula (21) it is possible to use dependence:

$$C \geq P_{max} \frac{\left(\gamma^2 + \gamma \cdot tg(\varphi_L)\right)}{2 \cdot \omega \cdot \varepsilon_{U_{DC}} \cdot U^2_{DC(REF)}} \tag{23}$$

In practice, from attention onto intermediate states as well as non-linearity of load, one should choose larger C capacity than results from dependences (21) and (23). Detailed analysis of this of problem, connected with proprieties of U_{DC} voltage regulator goes beyond frame of present paper.

In situation when system (network) voltage U_1 is not sinusoidal (poses higher harmonics or/and other components), to avoid source current distortion, there is need to use extended control algorithm (Fig. 6). The extended part has to extract the unneeded components (higher harmonics or/and other) from distorted network voltage U_1 and then add to the already shifted basic component (at frequency 50/60 Hz) of the supply voltage. This solution unfortunately leads to distorted load voltage. The decision about turning on the extended algorithm must be made after answer the question: what is more important sinusoidal source current, near unity input power factor and no overcurrents during source voltage sags and dips (when algorithm is on) or sinusoidal load voltage, great input reactive power and overcurrents during source voltage sags and dips (when algorithm is off)?

Table 1. Parameters of the investigated system

Source voltage	U_1	80 V
DC link reference voltage	$U_{DC(REF)}$	180 V
Series inductance	L_S	10.4 mH
Filter inductance	L_{f2}	0.3 mH
Filter capacitance	C_{f2}	24 μF
DC link capacitance	C	2000 μF
Switching frequency	f_1	10 kHz

3.2. Experimental results

To verify properties of the proposed parallel 1-phase VPLC (Fig. 5) a down scale hardware model, with parameters presented in Table 1, were developed.

On oscillograph records from Figure 7 to Figure 10 there are present experimental waveforms obtained for two different load types, linear (resistive) and non-linear (two pulse rectifier with capacitor filter).

Figure 7 illustrates investigated system behaviour in situation of linear (resistive) load. It is seen from this figure that VPLC influence on source current is on slight degree and can be additionally diminished through extended control algorithm (because of distorted supply voltage).

Figure 8, Figure 10 demonstrates the filtering capability of the VPLC. As one can see from those figures, the load current contains a large amount of harmonics due to two pulse rectifier with capacitor filter, however the source current is sinusoidal. The extended control algorithm can additionally improve shape of the source current because of distorted source voltage. Additionally in Table 2 and Table 3 are presenting THD coefficients in characteristic points of the both control algorithms.

Figure 10 demonstrates extended control algorithm properties in situation of source voltage magnitude variations. It is observed from those figures that in situation of nominal source voltage, algorithm generates only signal ($DU_{C(REF)}$) proportional to the higher harmonics in supply voltage. In situation when source voltage magnitude vary (magnitude under nominal value 3%) algorithm generates additionally basic frequency component. This procedure makes impossible occurrence overcurrents during voltage dips and sags as well as avoids input reactive power growth (see Figure 4).

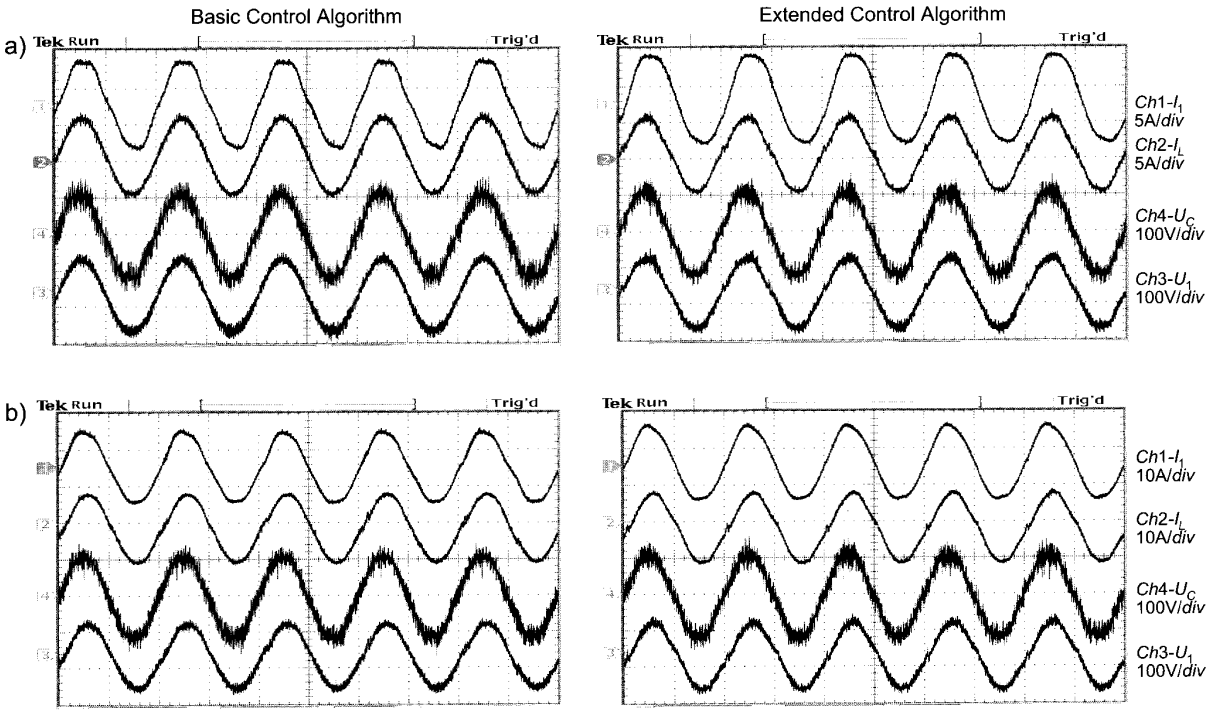

Fig. 7. Experimental waveforms (Δt = 10 ms/*div*) for linear load: a) $P_L = 0.4$ [kW]; b) $P_L = 1$ [kW]

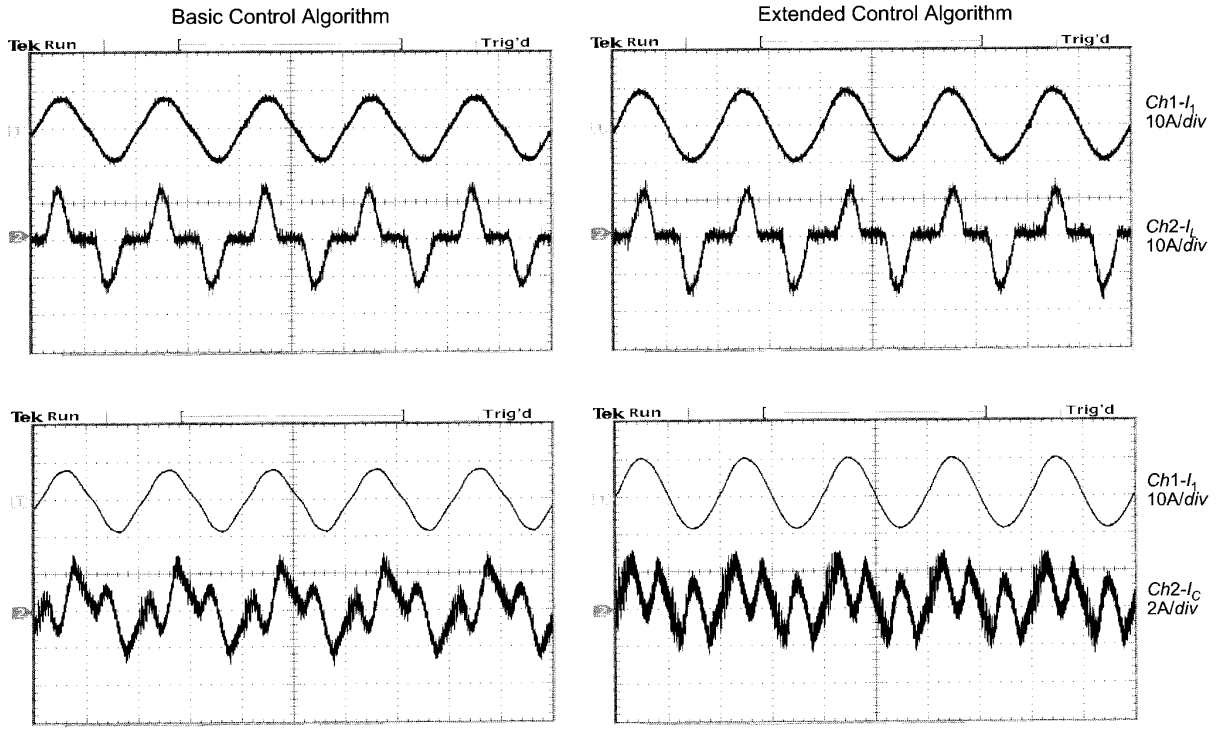

Fig. 8. Experimental waveforms (Δt = 10 ms/*div*) for non-linear load $P_L = 1$ [kW], where: I_C – VSI output current

3.3. Additional solutions

Variable input power factor problem can be solved in several ways. Constant and unity input power is possible to get in situation when VSC output voltage magnitude U_C is higher than source voltage magnitude U_1. For this purpose conditioner has to be equipped with additional source to supply to the DC link capacitor required active power.

The first additional solution is a conditioner with additional parallel connected current source (symmetrical configuration) as it is in Figure 11. In this case, to get unity input power factor, parallel current source (ΔI_1) has to produce

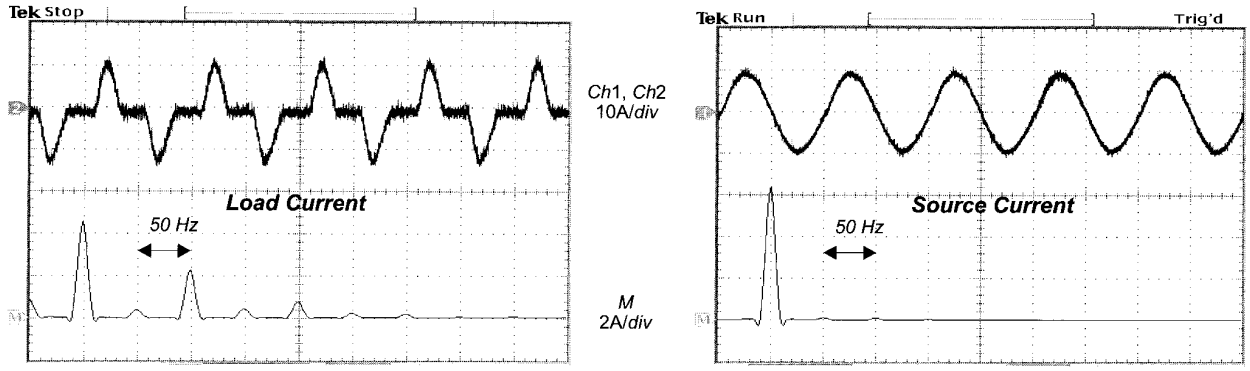

Fig. 9. Experimental waveforms (Δt = 10 ms/*div*) and spectrums for non-linear load P_L=1 [kW] (extended control algorithm)

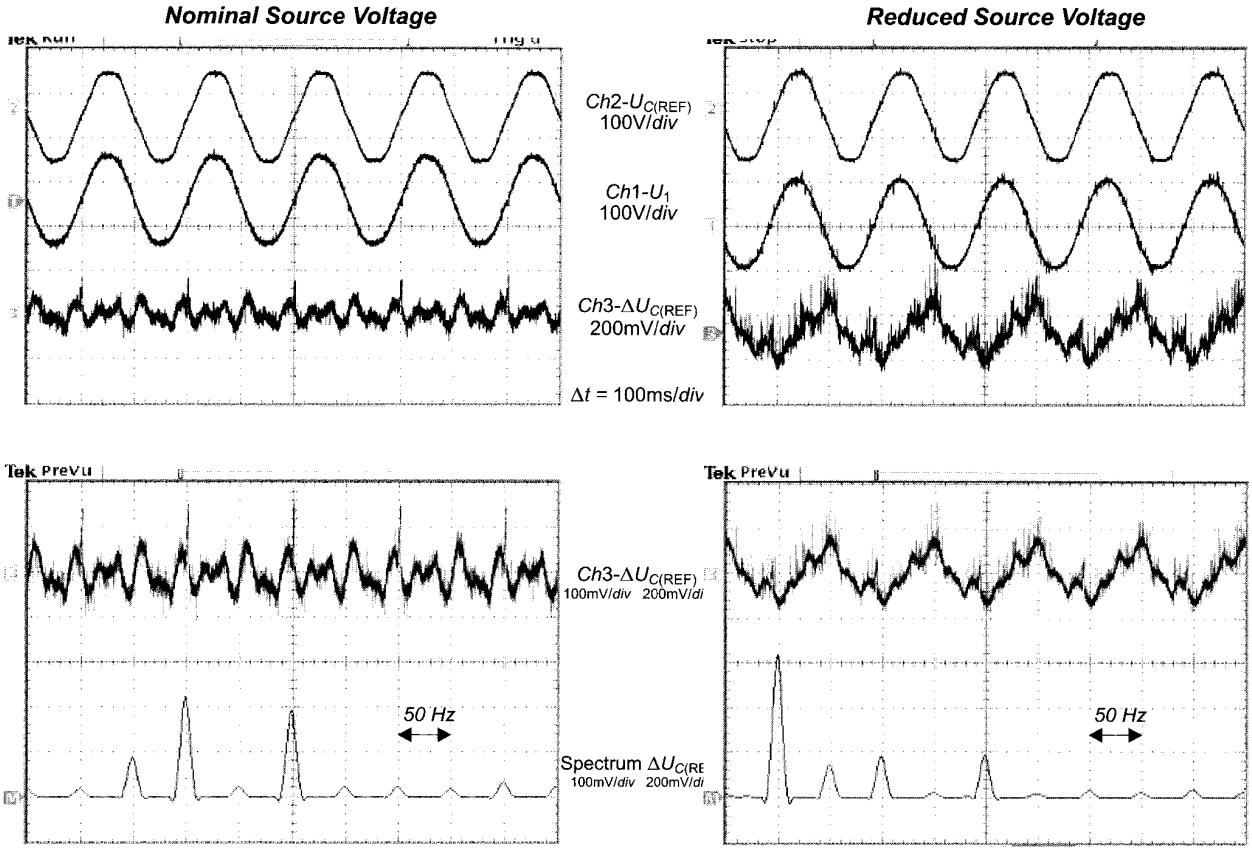

Fig. 10. Extended control algorithm performance in case of source voltage magnitude variations for non-linear load P_L = 1 [kW]

Table 2. THD coefficients in case of usage of basic control algorithm

Load		*THD* [%]			
		THD(I_1)	*THD*(U_1)	*THD*(I_L)	*THD*(U_L)
Linear	0.4 [kW]	13.7	3.6	2.8	4.5
	1 [kW]	7.9	5.6	4.4	9.1
Non-linear	0.4 [kW]	11.2	5.1	60.0	8.0
	1 [kW]	7.7	5.2	44.0	8.6

Table 3. THD coefficients in case of usage of extended control algorithm

Load		*THD* [%]			
		THD(I_1)	*THD*(U_1)	*THD*(I_L)	*THD*(U_L)
Linear	0.4 [kW]	9.9	6.1	6.3	7.7
	1 [kW]	5.9	9.2	5.9	15.6
Non-linear	0.4 [kW]	3.5	6.1	60.8	8.6
	1 [kW]	5.3	6.6	45.0	8.8

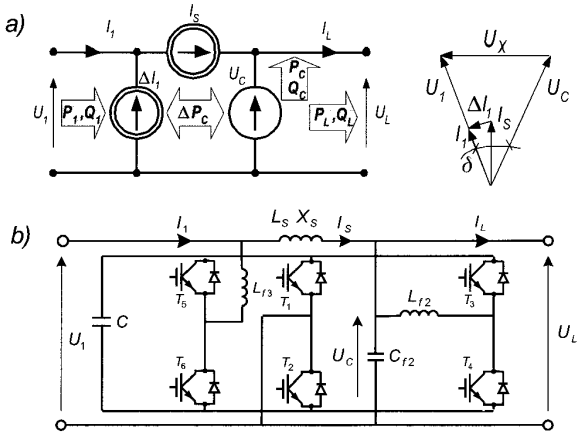

Fig.11. Symmetrical 1-phase VPLC: a) model; b) circuit

reactive current I_{Lf3} with proper magnitude, additionally implementing appropriate control algorithm (neglecting input power factor) there is possible to stabilize load voltage independent with source voltage variations. Because both parallel current source (ΔI_1) and parallel voltage source (U_C) possess common DC link capacitor there is also possible to exchange between them some active power and in this way avoid turn on mode problems and make U_C voltage stiffer.

The second solution is a conditioner with additional series connected voltage source, as it is in Figure 12. Implementing appropriate control algorithm (neglecting input power factor) there is also possible to stabilize load voltage independent with source voltage magnitude variations. In this system also unity input power factor is possible to get through changes of the active and reactive power flow. Equations on the active and reactive powers generated VSC are as follows:

$$P_C = P_L - \frac{U_C U_1}{X_S}\sin(\delta) - \underbrace{\frac{U_C \cdot \Delta U_{Sq}}{X_S}\cos(\varphi_2)}_{\equiv \Delta P_S} - \underbrace{\frac{U_C \cdot \Delta U_{Sp}}{X_1}\sin(\varphi_2)}_{\equiv \Delta P_C} \quad (24)$$

$$Q_C = \frac{U_C^2}{X_S} - \frac{U_C U_1}{X_S}\cos(\delta) - \underbrace{\frac{U_C \cdot \Delta U_{Sp}}{X_S}\cos(\varphi_2)}_{\equiv \Delta Q_C} + \underbrace{\frac{U_C \cdot \Delta U_{Sq}}{X_S}\sin(\varphi_2)}_{\equiv \Delta Q_S} + Q_L \quad (25)$$

where:

$\delta \angle(\vec{U}_1, \vec{U}_C)$,

$\varphi_2 \angle(\vec{I}_1, \vec{U}_C)$.

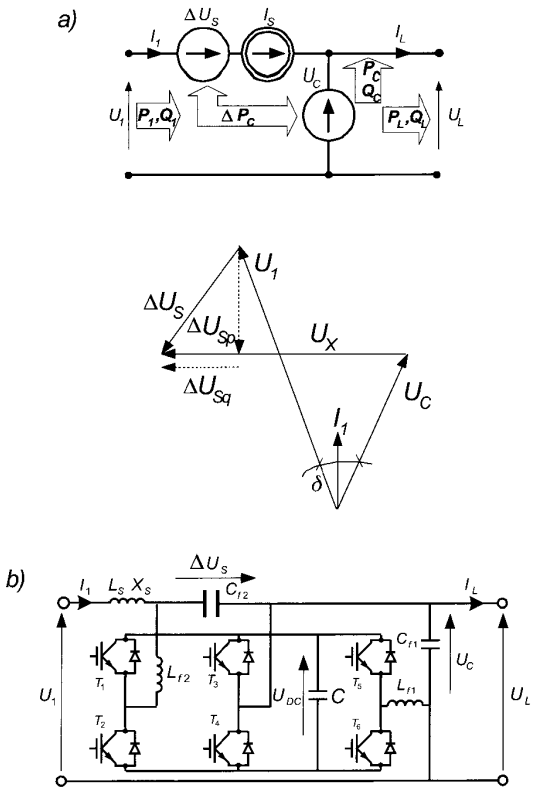

Fig. 12. Series-parallel 1-phase VPLC: a) model; b) circuit

It is known that series quadrature voltage injection U_{Sq} primarily affect the active power flow ΔP_S (in slight degree there is also affected reactive power flow ΔQ_S). Respectively series voltage injection U_{Sp} primarily affect the reactive power flow ΔQ_C (in slight degree there is also affected active power flow ΔP_C) [6, 8, 9]. Because series connected source internally can produce only voltage in quadrature with the line current, to produce in-phase voltage (to produce ΔP_C and ΔQ_C components) there is need additional source. This purpose is achieved with common, for both sources (series voltage and parallel voltage), DC link capacitor.

4. VPLC - 3-PHASE SOLUTIONS

Because multilevel converters can produce output voltage waveform having large number of steps, near-sinusoidal, they are the perfect solution for utilization in described VPLC system.

4.1. Four level cascade based VSC

Figure 13 presents proposed multilevel converter which is a series connection of the three 1-phase converter bridges (T1-T4) (T1'-T4') (T1"-T4") with the 3-phase converter bridge (T5-T6; T5'-T6'; T5"-T6"). Proposed converter can work in three- as well as four-line nets; in last case the DC supply capacitor on the three-phase inverter bridge has to be divi-

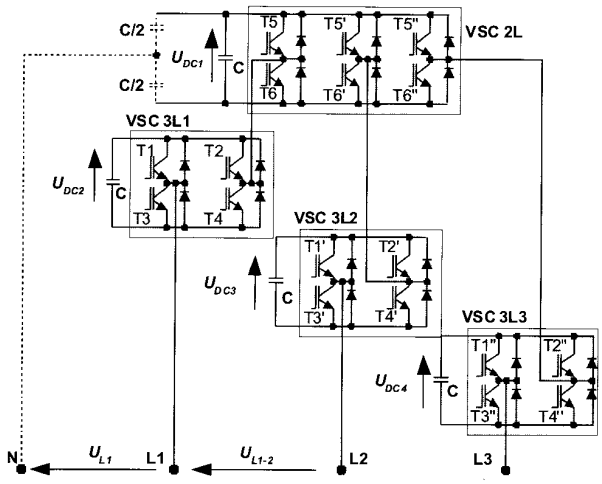

Fig.13. Proposed four level cascade based VSC

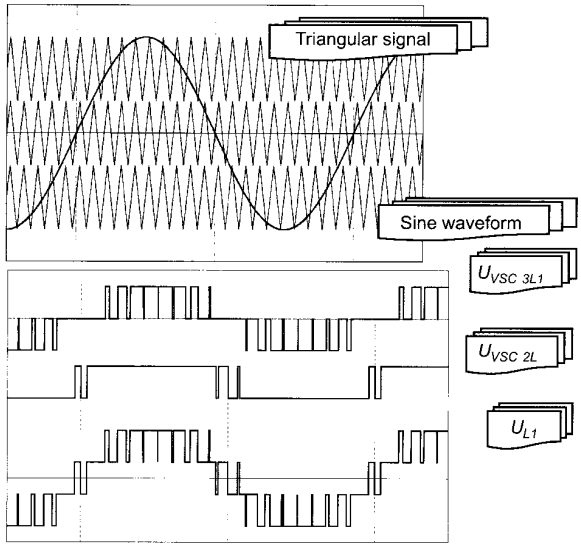

Fig. 14. Example of phase voltage forming in multilevel VSC

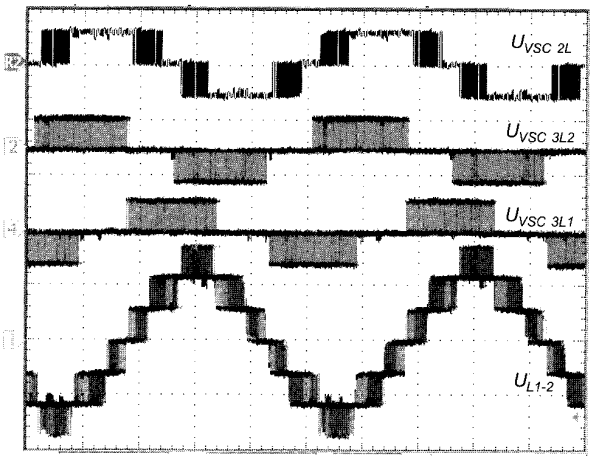

Fig. 15. Experimental results of the proposed multilevel VSC (ΔU = 500 V/*div*, Δt = 4 ms/*div*)

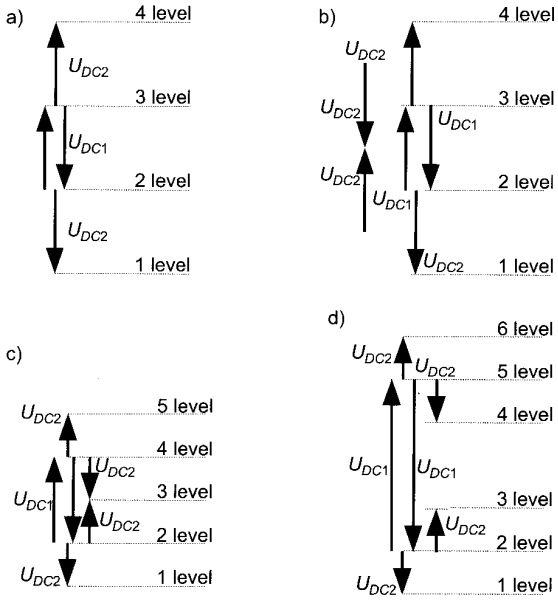

Fig. 16. Feasible phase voltage construction in proposed multilevel converter

ded, to create zero point. The major advantage of this topology lies in modularity, relatively simple construction and relatively simple way of avoidance problems of unbalanced voltages on DC link capacitors. A multilevel carrier based PWM was used, where for N-level inverter uses a set of N-1 triangular carrier waves with the same peak-to-peak magnitude and the same frequency.

Figure 14 presents, four-even-level quasi-sinusoidal phase output voltage (because U_{DC1}=U_{DC2}, for phase L1), on the cascade based converter, one can see that this voltage is a geometrical sum of voltages respectively on converter VSC 2L and VSC 3L1. Additionally, Fig.15 shows experimental results.

On the base of presented in Fig.13 cascade based multilevel inverter topology, it is also possible to get more than four level phase voltage. So far voltages on DC link capacitors were even U_{DC1}=U_{DC2}, then, for example in phase L1, output voltage was a geometrical sum of voltages respectively on converters VSC 2L and VSC 3L1. In situation of different DC link voltages and applying control algorithm, which makes possible both summation as well as subtraction voltages, it is possible to shape five- and even six-level phase voltage. Fig.16 shows phase voltage construction in situation of even and different DC voltages. On the base of Fig.16 we can see that in situation when DC link voltages are even U_{DC1} = (U_{DC2}; U_{DC3}; U_{DC4}) cascade topology based converter shapes 4 level phase voltage, additionally in situation when U_{DC1}=(2×U_{DC2}; 2×U_{DC3}; 2×U_{DC4}) and applying appropriate control algorithm converter shapes 5 level phase voltage and finally when U_{DC1}=(4×U_{DC2}; 4×U_{DC3}; 4×U_{DC4}) and with appropriate control algorithm inverter shapes 6 level phase voltage.

As it was told earlier, in this paper, changes of the d angle have an impact on the real power absorbed or supplied by

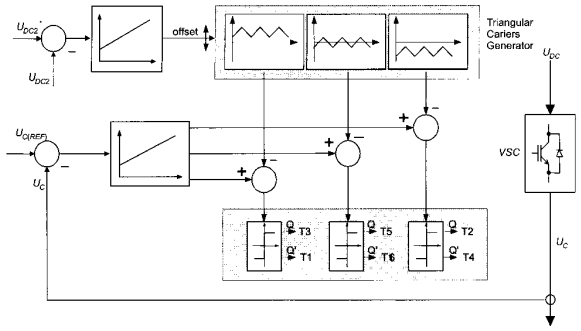

Fig. 17. Control algorithm of the four level cascade based VSC (phase L1)

the VSC thus there is possible the total DC link capacitors voltage regulation, however to avoid problem of unbalanced voltages the control algorithm has to be equipped with additional part, see Figure 17. First part, in the control algorithm, stabilizes voltage on the load at the reference value by means of a closed-loop control error between the measured voltage U_C and the reference voltage $U_{C(REF)}$. Second part secures constant U_{DC2}, U_{DC3}, and U_{DC4} voltages as a result of variable switching strategy of the transistors [4, 5]. Changed switching strategy can be reached adding suitable constant component to the triangular carriers (this does not cause changes on converter's output voltages and currents). The required constant component can be received from comparison the reference voltage, in L1 phase that will be U_{DC2}^*, with the actual measured value, in L1 phase that will be U_{DC2}. Received in this manner constant component shifts the triangular waves and in this way changes switching strategy what finally leads to DC link voltages equalization.

4.2. Experimental results

To verify results of the theoretical investigations a down scale multilevel VPLC hardware model, with parameters presented in Table 4, was developed. During investigations DC link voltages were even $U_{DC1} = U_{DC2} = U_{DC3} = U_{DC4}$ and on output of the cascade based four level VSC a Γ passive filter was implemented.

Table 4. Parameters of the investigated system

Source voltage	U_1	80 V
DC link reference voltage	U^*_{DC}	70 V
Series inductance	L_S	5.4 mH
Filter inductance	L_{f2}	0.3 mH
Filter capacitance	C_{f2}	18 μF
DC link capacitance	C	2200 μF
Switching frequency	f_l	10 kHz

Figure 18 – Figure 22 present experimental waveforms, during steady state operation of the multilevel VPLC, for two different load types, linear (*R-L* load) and non-linear (6-pulse rectifier with *R-L* load).

Figure 18 illustrates investigated VPLC's behaviour in situation of linear *R-L* load, *R=20* [W] and *L=72* [mH]. It is seen from this figure that multilevel VPLC has meaningful influence on the source current, distortions, in which, mostly come as result of the distorted supply voltage, see Figure 19 (basic control algorithm was implemented).

Above figure illustrates also the reactive power compensation capability. One can see from this figure that the load current lags the source voltage by about 35 degrees, however, the source current is almost in phase with the source voltage.

Additionally Figure 20 demonstrates VPLC's possibility for balancing the unbalanced loads in conditions of balanced source. Because VPLC produces sinusoidal balanced voltages, therefore source currents, in conditions of balanced power system, are also balanced. This condition, whether the load currents are balanced or not, is satisfied because the source currents are only determined by the source voltages, the VSC's output voltages as well as series reactance X_S, therefore we can claim that conditioner has peculiarity of balancing source in conditions of the unbalanced load. However in conditions of the unbalanced loads, currents produced by the VSC are also unbalanced what results in 100Hz component on the DC link voltages, the magnitude of which is proportional to the negative sequence of the load current.

Figure 21 demonstrates the filtering capabilities of the multilevel VPLC's. As one can see from those figures, the load

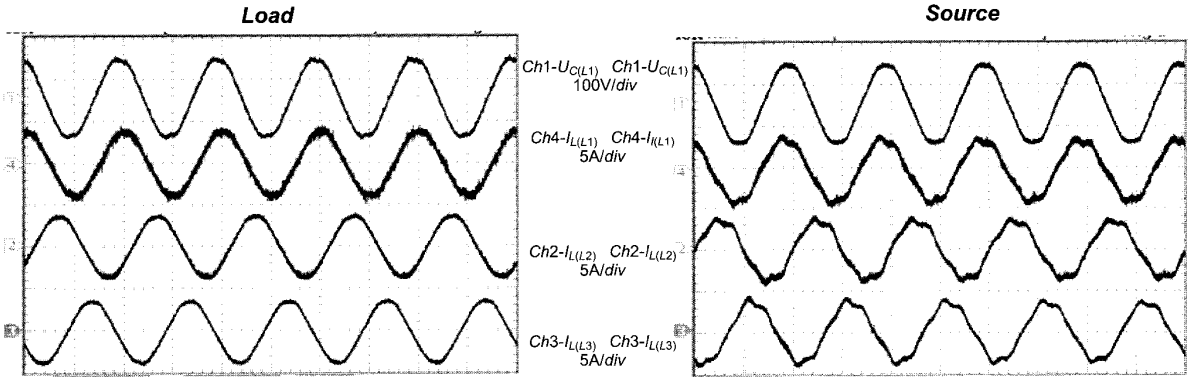

Fig. 18. Experimental waveforms obtained in 3-phase VPLC system (Δt = 10 ms/*div*) for linear load

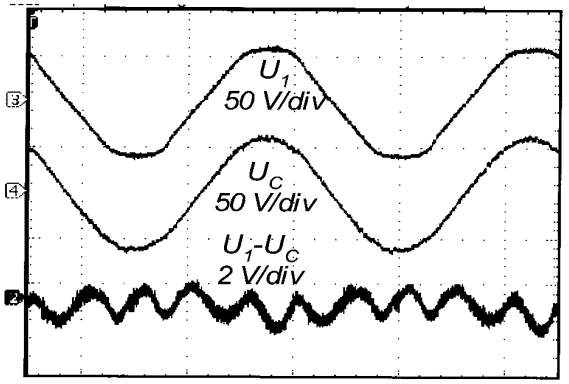

Fig. 19. Experimental results obtained in 3-phase VPLC system: source voltage U_1; VSC output voltage U_C; difference $U_1 - U_C$

current contains a large amount of harmonics due to the six pulse rectifier with resistive-inductive load; however the source current is almost sinusoidal (see Fig.21). Additionally Table 5 presents the THD coefficients in characteristic points of the investigated 3-phase VPLC's.

As it was told earlier, in the paper, VPLC, with described control algorithm, is "sensitive" on supply voltage variations (sags, dips), one can see from Fig.12. that those variations have impact on nature of the source current, in our case, because of source voltage magnitude is over it's nominal value, becomes more inductive.

Table 5. Investigated 3-phase VPLC and it's THD coefficients

		THD [%]			
		THD(I_I)	THD(U_I)	THD(I_L)	THD(U_L)
Non-linear load	P_L = 0.8[kW]	3.3	3.3	25.3	2.9
	P_L = 1.2[kW]	2.6	3.5	24.2	3.7

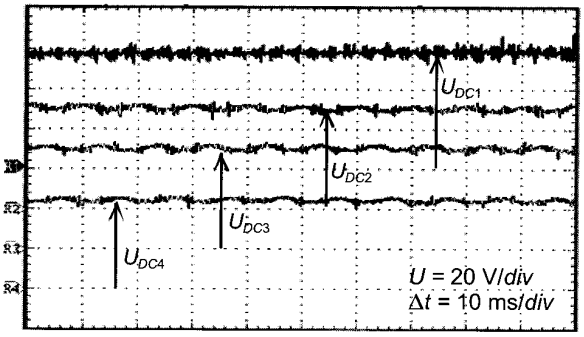

Fig. 22. Experimental results of the DC- link voltages for the 4-level VPLC

Additionally, Fig.22 demonstrates, in conditions of the non-linear load, four level cascade based VSC's DC link voltages.

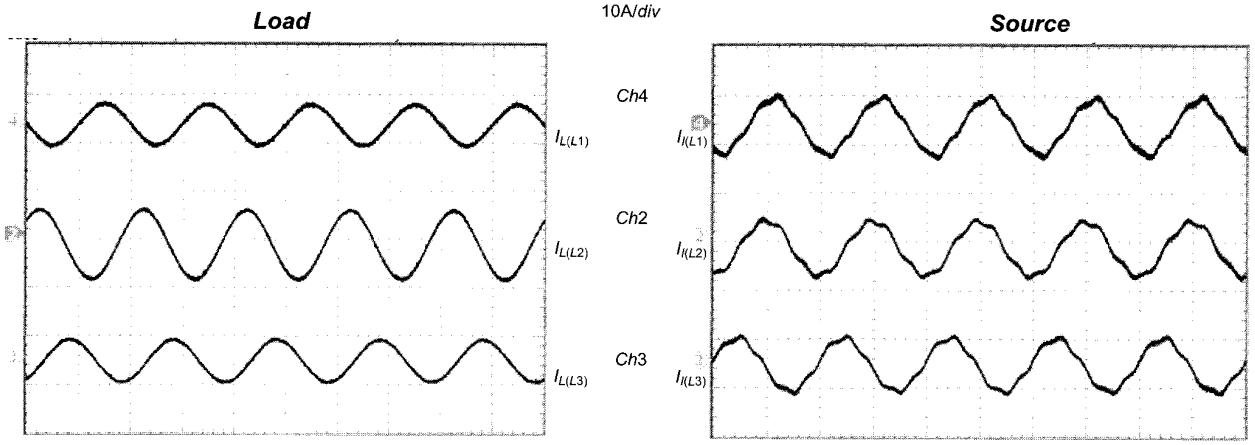

Fig. 20. Experimental waveforms of currents in 3-phase VPLC system (Δt = 10 ms/*div*) for linear unbalanced load

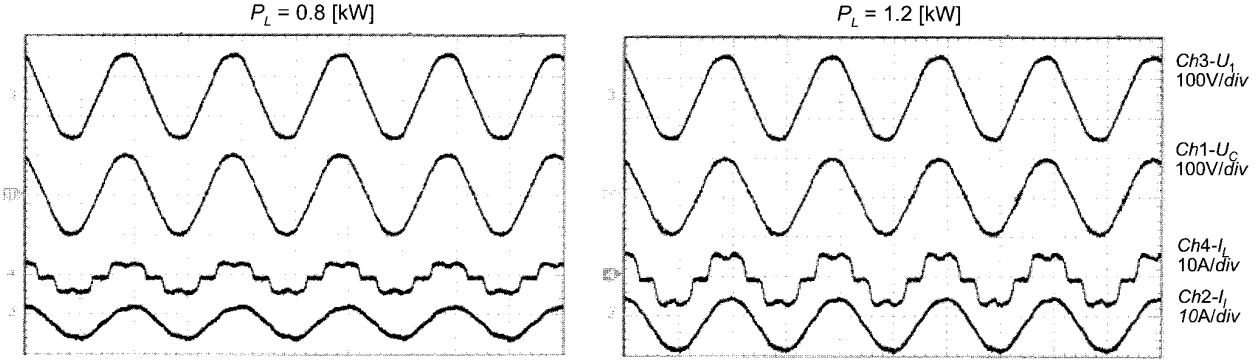

Fig. 21. Experimental waveforms (Δt = 10 ms/*div*) of 3-phase multilevel VPLC's in case of non-linear balanced load

5. CONCLUSIONS

Paper presents 1-phase and 3-phase Voltage Source Power Line Conditioners (VPLC), which permits to fulfill various tasks. There are additional significant advantages of VPLC, in comparison with APF systems, such as: voltage not current forming; very good filtration properties for any nonlinear load; possibilities of application of the simply line reactor L_S, which could be solely selected for fundamental frequency 50/60Hz.

Onto needs of the VPLC in 3-phase networks, four-level cascade based voltage converter was developed. To verify properties of the proposed conditioners a down scale hardware models have been developed. On the base of experimental investigations one can say that:

— VPLC's can free from higher harmonics source current, even in situation of strongly deformed load current; source current wave shape, in conditioners with extended control algorithm, is with source voltage wave shape independent;

— conditioners posses the load voltage stabilization in situation of source voltage magnitude variations; load voltage stabilization in conditions of the source voltage magnitude variations leads to the input reactive power growth, except for circuits presented on the Fig.11 and, in particular, Fig,12;

— three-phase VPLC circuit possess the capability of balancing the unbalanced loads in conditions of balanced source;

— to avoid problem of the source voltage shape influence on the filtration quality, control algorithm has to be equipped with low pass filter to check source voltage harmonics.

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