VOLTAGE SOURCE POWER LINE CONDITIONERS

Napięciowe kondycjery energii

Ryszard STRZELECKI
Maritime University of Gdynia

Grzegorz Benysek
Marcin JARNUT
Emil KOT
University of Zielona Góra

Summary: The paper presents a different way for a power quality conditioning. The different way means parallel connection of the sinusoidal voltage source with the network, therefore it is possible to "isolate" load from source and vice versa. Described conditioner makes possible to get: i) sinusoidal source current; ii) reactive power compensation; iii) load voltage stabilization; iv) balanced source in conditions of the unbalanced load (in 3-phase networks). As a sinusoidal voltage source in 3-phase network, the four level cascade based Voltage Source Converter (VSC) has been used. The effectiveness of the Voltage Source Power Line Conditioners (VPLC) is carefully outlined, while the systems general performance and flexibility are intensively investigated. To confirm results of the theoretical analysis some experimental results were presented.

Streszczenie: W artykuł opisano innny sposób poprawy jakości energii. Innny sposób oznacza tutaj równoległe połączenie z siecią źródła napięcia sinusoidalnego w wyniku czego możliwa jest „izolacja” obciążenia od sieci i vice versa. Opisany kondygnjer umożliwia uzyskanie: i) sinusoidalnego prądu sieci; ii) kompensacji mocy biernej; iii) stabilizacji napięcia na obciążeniu; iv) symetrizacji sieci w przypadku niesymetrycznego obciążenia (w sieciach 3-fazowych). Jako źródło napięcia sinusoidalnego, w sieciach 3-fazowych, wykorzystano kaskadowy czteropoziomowy falownik VSI. W artykule zbadano skuteczność Napięciowego Kondygnera Energii (VPLC) oraz opisano jego podstawowe właściwości. Wyniki analizy teoretycznej zostały poparte wynikami badań eksperymentalnych.

Keywords: power quality, active line conditioners, voltage source converter, multilevel converter, current harmonic compensation, reactive power compensation

Słowa kluczowe: jakość energii, aktywne kondycjery, falownik napięcia, falownik wielopoziomowy, kompensacja harmonicznych prądu, kompensacja mocy biernej

1. INTRODUCTION

The goal of this paper is to present simple, VPLC systems and to investigate, which extent they are suited to fulfill a wide range of different tasks:
— to prevent "dirty" loads from polluting the electrical distribution network (current conditioning mode);
— to protect sensitive loads from line disturbances as voltage sags (voltage restoring mode).

The intention is to combine circuit simplicity with flexibility in performance.

In professional literature [1, 2, 6, 7] there are described many different ways how to "isolate" sources from disturbances introduced by the nonlinear loads and vice versa.

For example to compensate higher harmonics of the current, produced by the nonlinear loads, Active Power Filters (APF) can be used [1, 2]. In those systems (independent with control algorithm) there is need to extract compensating components, from measured load or source currents (it depends if control algorithm is in open or closed loop), therefore the filtration quality is as good as it is possible to extract compensating components and shape them.

The paper presents a different way of a power quality improvement. In a presented solution there is no need to measure load or source currents, or to extract any compensating components, power quality improvement is possible using parallel connected VSC acts as a sinusoidal, with fundamental frequency, voltage source [3], therefore described conditioner makes possible to get:

This work was supported by the Polish Committee for Scientific Research under Grants 8T10A 01820
— sinusoidal source current;
— reactive power compensation;
— load voltage stabilization;
— balanced source in conditions of the unbalanced load (in 3-phase networks).

Because conditioner has to “produce” sinusoidal, with fundamental frequency, VSC are the perfect solution in this case. Onto needs of the Voltage Power Line Conditioners (VPLC) in 3-phase networks, the four-level cascade based voltage source inverter was developed [4, 5].

The paper consists of three major parts. First, Voltage Source Power Line Conditioner with special regard to current conditioning and the reactive power compensation mode in chapter 2 – will be explained. Chapter 3 presents 1-phase VPLC solutions. This chapter also includes enhanced controls algorithm and experimental results for 1-phase VPLC. The presentation of the major properties and experimental results of the four level cascade based VSC, in chapter 4 will be finally demonstrated.

2. VPLC – BASIC PROPERTIES

2.1. General property

Figure 1 shows a simplified scheme of the investigated VPLC and it’s control algorithm. The major difference between this conditioner and the others lies in the way of source current harmonics compensation. The “classic” conditioner has to detect the load current harmonic and generate the compensating components [1, 2]. Presently investigated system does not need to detect the load current harmonics, because they are naturally absorbed by the VSC, which has the attribute to “isolate” the load from the source (power system) [3].

In control algorithm PLL generates signal $U_{\text{CTRLP}}$ whose frequency is equal to that of the network and phase is shifted in relation to $U_1$ with angle $\delta$. Block A stabilizes voltage on the load at the reference value by means of a closed-loop control error between the RMS $U_C$ and the reference voltage $U_{\text{CTRLP}}$. To keep total DC link voltage on constant value PI controller was implemented.

Described conditioner consists of two major elements: series reactance $X_S$ (in first approximation represented by current source $I_S=I_1$) and controlled sinusoidal voltage source $U_{\text{CTRL}}$, both inserted between the source and the load. In situation when voltage $U_{\text{CTRL}}$ generated by the inverter, is shifted, in regard to the network voltage $U_1$, with angle $\delta$, there is possible power flow from source to load and source current $I_1$ becomes sinusoidal.

2.2. Harmonics suppression

The equivalent circuits of the VPLC at different conditions are presented in Figure 2. In those circuits $X_{CT}$ represents series reactance for fundamental frequency; respectively $X_{CB}$ represents series reactance for higher harmonics. $U_C$ and $U_1$ are respectively the fundamental part of the VSI output voltage and source voltage. Additionally $I_{CL}$ represents fundamental part of the load current and $I_{LH}$ higher harmonics of the load current.

As we can see, from Figure 2b for higher harmonics, because source voltage is sinusoidal therefore VSI produces also shifted sinusoidal component with fundamental frequency, both voltage sources $U_1$ and $U_C$ can be neglected and because $X_{SB}>>\delta$, load current is given by:

$$I_{LH} = I_{CH}$$

Therefore, the compensation characteristics to load can be written as:
On the base of above we can tell that considered conditioner provides "perfect" compensation of the load current higher harmonics, the voltage \( U_C \) generated by the VSC has the effect of "isolating" source from the non-linear loads.

2.2. Reactive power compensation

Proposed arrangement (Fig. 1) makes also possible reactive power compensation. Let us determine equation on input power factor.

For defined voltages:

\[
\tilde{U}_1 = U_1\cos(\delta) + jU_1\sin(\delta)
\]

\[
\tilde{U}_L = \tilde{U}_C = U_C
\]

where: \( \Delta \tilde{U}(\tilde{U}_1, \tilde{U}_C) \)

equations on active and reactive powers are as follows:

\[
R_L = \frac{U_L U_C}{X_S} \sin(\delta) \quad Q_L = \frac{U_L^2}{X_S} - \frac{U_L U_C}{X_S} \cos(\delta)
\]

\[
P_C = P_L - \frac{U_C U_1}{X_S} \sin(\delta)
\]

\[
Q_C = \frac{U_C^2}{X_S} - \frac{U_C U_1}{X_S} \cos(\delta) + Q_L
\]

where: \( P_L \) active and \( Q_L \) reactive power determined for \( U_L \) voltage and load parameters.

On the base of above equations, with assumption that \( U_1 = U_C \) and taking into account that in steady-state there is no active power exchange with VSI, i.e. \( P_1 = P_L \) and \( P_C = 0 \), equation on input power factor is as follows:

\[
PF_L = \cos\left(0.5\arcsin\left(\frac{P_L X_S}{U_1^2}\right)\right)
\]

and active \( P_1 \) and reactive \( Q_1 \) power are equal:

\[
P_1 = \frac{U_1^2}{X_S} \sin(\delta) \quad Q_1 = Q_L = \frac{U_1^2}{X_S} [1 - \cos(\delta)]
\]

On the base of curves presented in Figure 3 there is possibility to say that due to small values of inductance \( L_5 \) the phase angle between voltages \( U_1 \) and \( U_C \) is very small and hence the phase angle between \( I_1 \) and \( U_1 \) is even smaller. As a result, the input power factor is near unity.

For purpose of the reactive power compensation the magnitude \( U_C \) has to be controlled to be equal to that of \( U_1 \), because any differences between them are leading to considerable growth of the input reactive power, see Figure 4. The same amplitudes can be achieved by adjusting the converter modulation index.

If amplitude \( U' \neq U_C = U_1 \) and angle \( \delta' \) is as follows:

\[
U_C = U_1 \sqrt{1 + \sin^2(\delta)} \cdot \delta' = \arcsin\left(\frac{\sin(\delta)}{\sqrt{1 + \sin^2(\delta)}}\right)
\]

then

\[
P_1 = N_1 = N_1 \frac{U_L U_C'}{X_L} \sin(\delta') = \frac{U_1^2}{X_L} \sin(\delta)
\]

In this case

\[
Q_1 = Q_1 = N_1 = N_1 \frac{U_1 U_C'}{X_1} \cos(\delta') = 0
\]

3. VPLC - 1-PHASE SOLUTIONS

3.1. Parallel VPLC system

Investigated 1-phase VPLC system, presented in Figure 5, makes also possible to get sinusoidal source current \( I_1 \), input power factor near unity and, in situation of sinusoidal source voltage, load voltage without deformations. In this circuit, a two level PWM modulation VSC as \( U_C \) voltage source was used. Figure 6 presents the block diagram of the simplified control algorithm of the 1-phase VPLC (Fig.6).

Ryszard Strzelecki and other: Voltage Source Power Line Conditioners
Fig. 4. Influence of the $U_C$ on input reactive power, where: $P_{1a} - P_{1b}$; $Q_{1a}$ - input reactive power when $U_1 = U_C$

Fig. 5. Single-phase parallel VPLC circuit

If real power supplied by the system is greater than the load demand, the surplus portion will be absorbed by the VSC and thus cause the DC link capacitor voltage to increase. If real power supplied by the system is less than the load demand, the DC link capacitor voltage will decrease. To regulate the DC link capacitor voltage a PI controller was used. This controller uses the error between the reference $U_{DC(REF)}$ and the actual DC voltage $U_{DC}$ as a feedback signal. The PI controller produces the phase angle $d$ to control the real power absorbed or supplied by the VSC thus regulates the DC link capacitor voltage.

In steady state (neglecting the losses in the VSC) the angle $d$ corresponds to the real power supplied by the network (the real power supplied by the network has to be equal to the real power of the load). In this case instantaneous power taken/delivered to the VSC arrangement does not contain constant as well as variable component and it changes in accordance with dependence:

$$p_C(t) = Q_c \sin(2\omega t + 2\delta)$$  \hspace{1cm} (13)

From here the variable component of the energy accumulated in capacitor $C$, of the DC circuit, express equation:

$$\Delta E = \int p_C(t) \, dt = -\frac{Q_c}{2\omega} \cos(2\omega t + 2\delta)$$  \hspace{1cm} (14)

On basis of dependence (14) as well as formula onto energy accumulated in capacitance in dependence on voltage we receive the following equation:

$$|\Delta E_{\text{max}}| = C \cdot \left( \frac{U_{DC(max)}^2}{U_{DC(max)}^2} - \frac{U_{DC(min)}^2}{U_{DC(min)}^2} \right) = \frac{Q_c}{\omega}$$  \hspace{1cm} (15)

where:
- $\Delta E_{\text{max}}$ — peak-to-peak value of changes of energy in DC circuit;
- $U_{DC(max)}$, $U_{DC(min)}$ — maximum and minimum value of voltage $U_{DC}$

Taking into account that:
- reference voltage value

$$U_{DC(REF)} = \left( U_{DC(max)} + U_{DC(min)} \right) / 2$$  \hspace{1cm} (16)

Fig. 6. Block diagram of the control algorithm of the 1-phase VPLC system
— relative amplitude of pulsation of voltage $U_{DC}$

$$
\varepsilon_{U_{DC}} = \Delta U_{DC}/U_{DC(REF)}
$$

(17)

where:

$$
\Delta U_{DC} = \left| U_{DC(max)} - U_{DC(min)} \right|/2
$$

(18)

equation (17) can be expressed as:

$$
|\Delta E_{max}| = Q_C/\omega = 2 \cdot C \cdot \varepsilon_{U_{DC}} \cdot U_{DC(REF)}^2
$$

(19)

With assumption, that VPLC system is loaded with linear load with $\cos(\phi_L)$ power factor, taking into account dependences (6) and (7), as well as fact, that in steady state $P_1 = P_L$, demand onto reactive power $Q_C$ of the VSI arrangement can be calculated from dependency:

$$
Q_C = P_{max} \left( 1 + S - \sqrt{1 - \gamma^2 + \gamma \cdot \tan(\phi_L)} \right)
$$

(20)

where:

$$
P_{max} = \frac{U_1 \cdot U_C}{X_S}, \quad S = \frac{U_C - U_1}{U_1}, \quad \gamma = \frac{P}{P_{max}}
$$

In this case, as it results from equations (19) and (20), DC circuit capacity can not be smaller as calculated on basis of inequality:

$$
C \geq P_{max} \left( 1 + S - \sqrt{1 - \gamma^2 + \gamma \cdot \tan(\phi_L)} \right)
$$

(21)

where:

$$
U_{DC(REF)} \geq \left[ \sqrt{2 \cdot (1 + S) \cdot U_1} \right]/(1 - 2 \cdot \varepsilon_{U_{DC}})
$$

(22)

In special case, when $U_C = U_1$ (i.e. $S = 0$) as well as relatively small load power (about $\gamma < 0.2$), instead of formula (21) it is possible to use dependence:

$$
C \geq P_{max} \left( \gamma^2 + \gamma \cdot \tan(\phi_L) \right)
$$

(23)

In practice, from attention onto intermediate states as well as non-linearity of load, one should choose larger C capacity than results from dependences (21) and (23). Detailed analysis of this of problem, connected with properties of $U_{DC}$ voltage regulator goes beyond frame of present paper.

In situation when system (network) voltage $U_1$ is not sinusoidal (posses higher harmonics or/and other components), to avoid source current distortion, there is need to use extended control algorithm (Fig. 6). The extended part has to extract the unneeded components (higher harmonics or/and other) from distorted network voltage $U_1$ and then add to the already shifted basic component (at frequency 50/60 Hz) of the supply voltage. This solution unfortunately leads to distorted load voltage. The decision about turning on the extended algorithm must be made after answer the question: what is more important sinusoidal source current, near unity input power factor and no overcurrents during source voltage sags and dips (when algorithm is on) or sinusoidal load voltage, great input reactive power and overcurrents during source voltage sags and dips (when algorithm is off)?

3.2. Experimental results

To verify properties of the proposed parallel 1-phase VPLC (Fig. 5) a down scale hardware model, with parameters presented in Table 1, were developed.

<table>
<thead>
<tr>
<th>Source voltage</th>
<th>$U_{DC(REF)}$</th>
<th>80 V</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC link reference voltage</td>
<td>$U_{DC(REF)}$</td>
<td>180 V</td>
</tr>
<tr>
<td>Series inductance</td>
<td>$L_s$</td>
<td>10.4 mH</td>
</tr>
<tr>
<td>Filter inductance</td>
<td>$L_0$</td>
<td>0.3 mH</td>
</tr>
<tr>
<td>Filter capacitance</td>
<td>$C_f$</td>
<td>24 µF</td>
</tr>
<tr>
<td>DC link capacitance</td>
<td>$C$</td>
<td>2000 µF</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>$f_s$</td>
<td>10 kHz</td>
</tr>
</tbody>
</table>

Table 1. Parameters of the investigated system

On oscillograph records from Figure 7 to Figure 10 there are present experimental waveforms obtained for two different load types, linear (resistive) and non-linear (two pulse rectifier with capacitor filter).

Figure 7 illustrates investigated system behaviour in situation of linear (resistive) load. It is seen from this figure that VPLC influence on source current is on slight degree and can be additionally diminished through extended control algorithm (because of distorted supply voltage).

Figure 8, Figure 10 demonstrates the filtering capability of the VPLC. As one can see from those figures, the load current contains a large amount of harmonics due to pulse rectifier with capacitor filter, however the source current is sinusoidal. The extended control algorithm can additionally improve shape of the source current because of distorted source voltage. Additionally in Table 2 and Table 3 are presenting THD coefficients in characteristic points of the both control algorithms.

Figure 10 demonstrates extended control algorithm properties in situation of source voltage magnitude variations. It is observed from those figures that in situation of nominal source voltage, algorithm generates only signal ($U_{DC(REF)}$) proportional to the higher harmonics in supply voltage. In situation when source voltage magnitude vary (magnitude under nominal value 3%) algorithm generates additionally basic frequency component. This procedure makes impossible occurrence overcurrents during voltage dips and sags as well as avoids input reactive power growth (see Figure 4).
3.3. Additional solutions

Variable input power factor problem can be solved in several ways. Constant and unity input power is possible to get in situation when VSC output voltage magnitude $U_C$ is higher than source voltage magnitude $U_I$. For this purpose conditioner has to be equipped with additional source to supply to the DC link capacitor required active power.

The first additional solution is a conditioner with additional parallel connected current source (symmetrical configuration) as it is in Figure 11. In this case, to get unity input power factor, parallel current source ($\Delta I_f$) has to produce
Fig. 9. Experimental waveforms ($\Delta t = 10$ ms/div) and spectrums for non-linear load $P_L = 1$ [kW] (extended control algorithm)

Fig. 10. Extended control algorithm performance in case of source voltage magnitude variations for non-linear load $P_L = 1$ [kW]

<table>
<thead>
<tr>
<th>Load</th>
<th>THD [%]</th>
<th>THD ($I_L$)</th>
<th>THD ($U_{I}$)</th>
<th>THD ($I_J$)</th>
<th>THD ($U_{J}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Linear</td>
<td>0.4 [kW]</td>
<td>13.7</td>
<td>3.6</td>
<td>2.8</td>
<td>4.5</td>
</tr>
<tr>
<td></td>
<td>1 [kW]</td>
<td>7.9</td>
<td>5.6</td>
<td>4.4</td>
<td>9.1</td>
</tr>
<tr>
<td>Non-linear</td>
<td>0.4 [kW]</td>
<td>11.2</td>
<td>5.1</td>
<td>60.0</td>
<td>8.0</td>
</tr>
<tr>
<td></td>
<td>1 [kW]</td>
<td>7.7</td>
<td>5.2</td>
<td>44.0</td>
<td>8.6</td>
</tr>
</tbody>
</table>

Table 3. THD coefficients in case of usage of extended control algorithm

<table>
<thead>
<tr>
<th>Load</th>
<th>THD [%]</th>
<th>THD ($I_L$)</th>
<th>THD ($U_{I}$)</th>
<th>THD ($I_J$)</th>
<th>THD ($U_{J}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Linear</td>
<td>0.4 [kW]</td>
<td>9.9</td>
<td>6.1</td>
<td>6.3</td>
<td>7.7</td>
</tr>
<tr>
<td></td>
<td>1 [kW]</td>
<td>5.9</td>
<td>9.2</td>
<td>5.9</td>
<td>15.6</td>
</tr>
<tr>
<td>Non-linear</td>
<td>0.4 [kW]</td>
<td>3.5</td>
<td>6.1</td>
<td>60.8</td>
<td>8.6</td>
</tr>
<tr>
<td></td>
<td>1 [kW]</td>
<td>5.3</td>
<td>6.6</td>
<td>45.0</td>
<td>8.8</td>
</tr>
</tbody>
</table>
reactive current $I_{f,0}$ with proper magnitude, additionally implementing appropriate control algorithm (neglecting input power factor) there is possible to stabilize load voltage independent with source voltage variations. Because both parallel current source ($\Delta I_f$) and parallel voltage source ($U_C$) possess common DC link capacitor there is also possible to exchange between them some active power and in this way avoid turn on mode problems and make $U_C$ voltage stiffer.

The second solution is a conditioner with additional series connected voltage source, as it is in Figure 12. Implementing appropriate control algorithm (neglecting input power factor) there is also possible to stabilize load voltage independent with source voltage magnitude variations. In this system also unity input power factor is possible to get through changes of the active and reactive power flow. Equations on the active and reactive powers generated VSC are as follows:

$$
P_{c} = P_{c0} - \frac{U_C U_i}{X_S} \sin(\delta) - \frac{U_C \Delta U_{s0} \cos(\varphi_2)}{X_S} \Delta P_i + \frac{U_C \Delta U_{s0} \sin(\varphi_2)}{X_S} \Delta P_i \quad (24)$$

$$
Q_{c} = \frac{U_C^2}{X_S} - \frac{U_C U_i}{X_S} \cos(\delta) - \frac{U_C \Delta U_{s0} \cos(\varphi_2)}{X_S} + \frac{U_C \Delta U_{s0} \sin(\varphi_2)}{X_S} + Q_{c0} \quad (25)$$

where:

$$\delta \angle (\bar{U}_i, \bar{U}_C),$$

$$\varphi_2 \angle (\bar{I}_i, \bar{U}_C).$$

It is known that series quadrature voltage injection $U_{s0}$ primarily affect the active power flow $\Delta P_S$ (in slight degree there is also affected reactive power flow $\Delta Q_S$). Respectively series voltage injection $U_{s0}$ primarily affect the reactive power flow $\Delta Q_C$ (in slight degree there is also affected active power flow $\Delta P_C$) [6, 8, 9]. Because series connected source internally can produce only voltage in quadrature with the line current, to produce in-phase voltage (to produce $\Delta P_C$ and $\Delta Q_C$ components) there is need additional source. This purpose is achieved with common, for both sources (series voltage and parallel voltage), DC link capacitor.

4. VPLC - 3-PHASE SOLUTIONS

Because multilevel converters can produce output voltage waveform having large number of steps, near-sinusoidal, they are the perfect solution for utilization in described VPLC system.

4.1. Four level cascade based VSC

Figure 13 presents proposed multilevel converter which is a series connection of the three 1-phase converter bridges (T1-T4) (T1'-T4') with the 3-phase converter bridge (T5-T6; T5'-T6'; T5''-T6''). Proposed converter can work in three- as well as four-line nets; in last case the DC supply capacitor on the three-phase inverter bridge has to be divi-
Fig. 13. Proposed four level cascade based VSC

Fig. 14. Example of phase voltage forming in multilevel VSC

Fig. 15. Experimental results of the proposed multilevel VSC ($\Delta U = 500\, \text{V/div}, \Delta t = 4\, \text{ms/div}$)

Fig. 16. Feasible phase voltage construction in proposed multilevel converter

...}

...
the VSC thus there is possible the total DC link capacitors voltage regulation, however to avoid problem of unbalanced voltages the control algorithm has to be equipped with additional part, see Figure 17. First part, in the control algorithm, stabilizes voltage on the load at the reference value by means of a closed-loop control error between the measured voltage $U_L$ and the reference voltage $U_{L_{REF}}$. Second part secures constant $U_{DC2}$, $U_{DC3}$, and $U_{DC1}$ voltages as a result of variable switching strategy of the transistors [4, 5]. Changed switching strategy can be reached adding suitable constant component to the triangular carriers (this does not cause changes on converter’s output voltages and currents). The required constant component can be received from comparison the reference voltage, in L1 phase that will be $U_{DC2}^{*}$, with the actual measured value, in L1 phase that will be $U_{DC2}$. Received in this manner constant component shifts the triangular waves and in this way changes switching strategy what finally leads to DC link voltages equalization.

### 4.2. Experimental results

To verify results of the theoretical investigations a down scale multilevel VPLC hardware model, with parameters presented in Table 4, was developed. During investigations DC link voltages were even $U_{DC1} = U_{DC2} = U_{DC3} = U_{DC0}$ and on output of the cascade based four level VSC a Γ passive filter was implemented.

<table>
<thead>
<tr>
<th>Table 4</th>
<th>Parameters of the investigated system</th>
</tr>
</thead>
<tbody>
<tr>
<td>Source voltage</td>
<td>$U_s$</td>
</tr>
<tr>
<td>DC link reference voltage</td>
<td>$U_{DC}$</td>
</tr>
<tr>
<td>Series inductance</td>
<td>$L_s$</td>
</tr>
<tr>
<td>Filter inductance</td>
<td>$L_2$</td>
</tr>
<tr>
<td>Filter capacitance</td>
<td>$C_2$</td>
</tr>
<tr>
<td>DC link capacitance</td>
<td>$C$</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>$f_s$</td>
</tr>
</tbody>
</table>

Figure 18 - Figure 22 present experimental waveforms, during steady state operation of the multilevel VPLC, for two different load types, linear (R-L load) and non-linear (6-pulse rectifier with R-L load).

Figure 18 illustrates investigated VPLC’s behaviour in situation of linear R-L load, $R = 20$ [W] and $L = 72$ [mH]. It is seen from this figure that multilevel VPLC has meaningful influence on the source current, distortions, in which, mostly come as result of the distorted supply voltage, see Figure 19 (basic control algorithm was implemented).

Above figure illustrates also the reactive power compensation capability. One can see from this figure that the load current lags the source voltage by about 35 degrees, however, the source current is almost in phase with the source voltage.

Additionally Figure 20 demonstrates VPLC’s possibility for balancing the unbalanced loads in conditions of balanced source. Because VPLC produces sinusoidal balanced voltages, therefore source currents, in conditions of balanced power system, are also balanced. This condition, whether the load currents are balanced or not, is satisfied because the source currents are only determined by the source voltages, the VSC’s output voltages as well as series reactance $X_S$, therefore we can claim that conditioner has peculiarity of balancing source in conditions of the unbalanced load. However in conditions of the unbalanced loads, currents produced by the VSC are also unbalanced what results in 100Hz component on the DC link voltages, the magnitude of which is proportional to the negative sequence of the load current.

Figure 21 demonstrates the filtering capabilities of the multilevel VPLC’s. As one can see from those figures, the load...
current contains a large amount of harmonics due to the six pulse rectifier with resistive-inductive load; however the source current is almost sinusoidal (see Fig.21). Additionally Table 5 presents the THD coefficients in characteristic points of the investigated 3-phase VPLC’s.

As it was told earlier, in the paper, VPLC, with described control algorithm, is “sensitive” on supply voltage variations (sags, dips), one can see from Fig.12, that those variations have impact on nature of the source current, in our case, because of source voltage magnitude is over it’s nominal value, becomes more inductive.

---

**Table 5. Investigated 3-phase VPLC and it’s THD coefficients**

<table>
<thead>
<tr>
<th>Non-linear $P_L = 0.8[kW]$</th>
<th>$P_L = 1.2[kW]$</th>
</tr>
</thead>
<tbody>
<tr>
<td>THD($I_L$)</td>
<td>THD($U_C$)</td>
</tr>
<tr>
<td>3.3</td>
<td>3.3</td>
</tr>
<tr>
<td>2.6</td>
<td>3.5</td>
</tr>
</tbody>
</table>

---

**Fig. 22. Experimental results of the DC-link voltages for the 4-level VPLC**

Additionally, Fig.22 demonstrates, in conditions of the non-linear load, four level cascade based VSC’s DC link voltages.

---

**Fig. 20. Experimental waveforms of currents in 3-phase VPLC system ($\Delta t = 10\ ms/div$) for linear unbalanced load**

**Fig. 21. Experimental waveforms ($\Delta t = 10\ ms/div$) of 3-phase multilevel VPLC’s in case of non-linear balanced load**
5. CONCLUSIONS

Paper presents 1-phase and 3-phase Voltage Source Power Line Conditioners (VPLC), which permits to fulfill various tasks. There are additional significant advantages of VPLC, in comparison with APF systems, such as: voltage not current forming; very good filtration properties for any nonlinear load; possibilities of application of the simply line reactor $L_0$, which could be solely selected for fundamental frequency 50/60 Hz.

Onto needs of the VPLC in 3-phase networks, four-level cascade based voltage converter was developed. To verify properties of the proposed conditioners a down scale hard-ware models have been developed. On the base of experimental investigations one can say that:

— VPLC’s can free from higher harmonics source current, even in situation of strongly deformed load current; source current wave shape, in conditioners with extended control algorithm, is with source voltage wave shape independent;

— conditioners passes the load voltage stabilization in situation of source voltage magnitude variations; load voltage stabilization in conditions of the source voltage magnitude variations leads to the input reactive power growth, except for circuits presented on the Fig.11 and, in particular, Fig.12;

— three-phase VPLC circuit possess the capability of balancing the unbalanced loads in conditions of balanced source;

— to avoid problem of the source voltage shape influence on the filtration quality, control algorithm has to be equipped with low pass filter to check source voltage harmonics.

6. REFERENCES


Ryszard Strzelecki

was born in Bydgoszcz, Poland, on September 28, 1955. He received his undergraduate education at the Technical-Agricultural Academy, Bydgoszcz, further studies at the Technical University, Kiev, Ukraine (M.S.E.E 1982, Ph.D. 1985). In 1992 he became an Assistant Professor at Technical Agricultural Academy, Bydgoszcz. In 1994 he became an Associate Professor and in 1999 a Professor at Technical University of Zielona Gora. From 1996 he is Manager of the Institute of Electrical Engineering at Technical University of Zielona Gora. Professor Strzelecki has a broad experience in all areas of power improvement and control, and has been pioneering, in Poland, advanced power electronic-based compensation and control techniques for utility applications for Zielona Gora. He received many awards. His areas of interest include electrical power quality improvement, particularly methods of reducing the influence of nonlinear loads on supply network, FACTS technologies. Professor is a member of several national and international committees, among others in IEEE, PELS/IES, PES, IAS.

Grzegorz Benysek

was born in Sulechow, Poland, on June 17, 1968. He received his undergraduate education at the Technical University of Zielona Gora (M.S.E.E 1994, Ph.D. 1998). Now he is a teacher in Institute of Electrical Engineering at University of Zielona Gora. His major research interest include analysis and control of power electronics circuits, control methods and properties investigations of the filtration systems as: active power filters, hybrid filters and series-parallel filters and other FACT Systems. His researches are also going in direction of utilization of the renewable energy sources in FACTS technologies.

Marek Jarnut

was born in Siewodzin, Poland, on November 29, 1974. He received M.Sc. degree from University of Zielona Gora in 2000. From 2002 he is working at University of Zielona Gora in Institute of Electrical Engineering. In 2003 he has started doctoral dissertation joining with power quality improvement using controlled voltage sources. His main research area includes power conditioning, high frequency power converters, switch mode power supplies.

Emil Kot

was born in 1974 in Kożuchów, Poland. He is received the M.Sc. degree from in the Technical University of Zielona Gora. Present he is researcher at the University of Zielona Gora. His research area include Multilevel Voltage Source Inverters, Active Power Filters and computer simulations of advanced electric drives. In 2002 he has started doctoral dissertation concerning analysis of the multilevel voltage source inverters based on cascade topology. He is an author of more than 28 papers on many international conferences, among other EPE, PESC, IAS.