Jakość i Użytkowanie Energii Elektrycznej
Tom X Zeszyt 1/2 Rok 2004

CRITICAL EVALUATION OF RESONANT DC VOLTAGE LINK INVERTERS FOR ELECTRICAL DRIVES

Krytyczna ocena falowników z centralnym obwodem rezonansowym dla napędów elektrycznych

Sławomir MANDREK
Gdańsk Shiprepair Yard "Remontowa" S.A.

Piotr J. CHRZAN
Gdańsk University of Technology

Summary: **This paper deals with modeling and simulation of resonant dc voltage link inverters for electrical drives applications. Different types of active clamped, parallel and quasi-resonant dc link structures are compared. Vis-a-vis contradictory objectives, selective and compromise evaluation is given.**

Streszczenie: **Przedstawiono wyniki modelowania i symulacji falowników z centralnym obwodem rezonansowym dla zastosowań w napędzie elektrycznym. Porównano struktury układów z rezonansowym równoległym obwodem pośredniczącym o ograniczonej wartości szczytowej i quasi-rezonansowych. Dla potrzeb projektowania tych układów, wobec przeciwstawnych funkcji celu, dokonano ich selektywnej i kompromisowej oceny.**

Keywords: EMI noise, resonant inverters, electrical drives
Słowa kluczowe: zakłócenia elektromagnetyczne, falowniki rezonansowe, napędy elektryczne

1. INTRODUCTION

Fundamental topology of voltage source inverters is usually based on bridge scheme, consisting of six bilateral switches with IGBT transistors. Usefulness of this class of converters is confirmed by a number of advantages, e.g.: relative simple topology, available modulation strategies, robust detection of failures, or fast commutation rates. But undesirable high voltage derivatives of power transistors, may provoke some harmful phenomena in electrical drives, such as:
— electromagnetic interference EMI emissions (conducted or radiated),
— increase of bearing currents,
— overvoltage spikes at motor terminals.

A solution to diminish these effects, as has been successfully described in a series of papers originated by Divan and others [7-10], particularly in application of the Active Clamped Resonant Direct Current Link Inverter ACRDCLI. The original idea points to insert a resonant circuit into dc link between line and machine converters (Fig. 1). The aim of which is a generation of pulse voltage of high frequency (dozens of kHz), limited commutation transients rate (hundreds of V/μs) and appropriate amplitude. Changing of switching pattern in the inverter bridge follows an instant when dc link voltage decreases resonantly to zero. As, continuous operation of resonant circuit is disadvantageous for control of inverter with the pulse width modulation PWM technique.

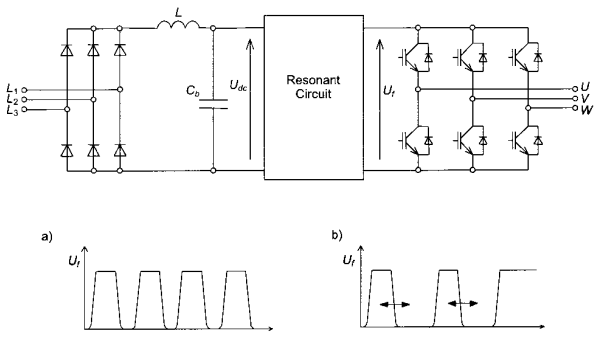

Fig.1. Frequency converter with resonant circuit input inverter voltage: a) ACRDCLI, b) QRDCLI

Hence, a number of new results have been obtained for the Quasi RDCLI, where initial instant of each one resonant cycle is commanded externally from microcontroller.

In this paper, is considered a critical evaluation and comparison of resonant dc voltage link inverters, which transparent schemes have been developed chronologically by Divan, Skibinski [8], Salama [3,14], Sul [5], Yoshitsugu [15], Kurokawa [12].

Systematic simulations with aid of the TCAD 6.0 circuit simulator enhance the study. For simplicity of simulation and without loss of resonant circuit topology, a full bridge inverter is represented by one bilateral switch: transistor Tf and free-wheel diode D_f (Fig.2). Dimensioning of the resonant circuit corresponds to the specific inverter unit (I_o = 60A, U_f= 160V, f= 30kHz). However to compare timing principles, a basic operation is simulated for zero load current. Off-line transistors gating for sensorless resonant circuit operation are applied, thus eliminating delicate current/voltage on-line detectors and comparators. Preliminary by simulation research are minimized passive LC elements.

Comparative research deals with resonant circuit complexity, commutation type of additional transistors, over current/voltage stress on circuit elements, sensitivity to motor current changes or reactive energy storage trajectories. Some particular circuit data concerning fall and rise voltage derivatives, zero link voltage periods and dimensioning of circuit elements are given in the third chapter of comparative evaluation.

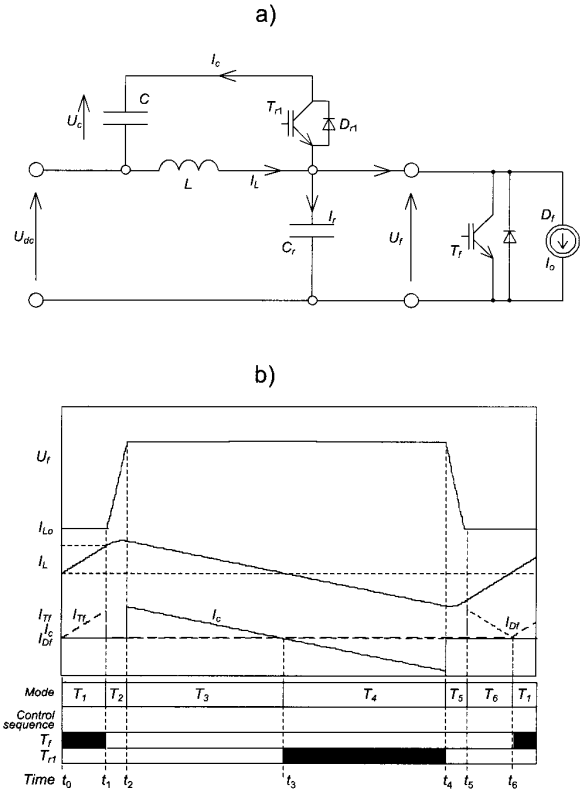

Fig.2. Active clamped resonant DC-link inverter; a) scheme, b) waveforms and gating sequences

2. INVESTIGATED TOPOLOGIES

2.1. Active clamped resonant DC-link inverter

The original active clamping technique was developed by Divan, Skibinski [8] to limit DC-link voltage resonant overshoots and its dependence of load current. The scheme diagram with simulation waveforms are depicted in Fig. 2.

The resonant cycle is initialised at t_0, when the transistor T_f is turned on. Then inductor current I_L increases linearly in the circuit consisted of voltage source U_{dc}, inductor L, transistor T_f. When current I_L reaches predetermined value I_{L0} at t_1, the transistor T_f is turned off. The inductor current I_L charges the capacitor C_r causing resonant build-up of DC-link voltage U_f. On reaching a voltage $U_{dc} + U_c$ at t_2, diode D_{r1} turns on and clamps the DC-link voltage, constituting the resonant circuit LC. While D_{r1} starts to conduct at t_2, transistor T_{r1} can be turned on, at least at t_3 to enable resonant recharging capacitor C. At instant t_4, when the negative inductor current reaches -IL0, transistor T_{r1} is turned off forcing inductor current I_L to recharged capacitor C_r until the DC link voltage U_f reaches zero. Then inverter diode D_f starts to conduct with increasing to zero inductor current. At this point the resonant cycle can be reinitiated.

Despite of original structure and defined sequences of operation, the circuit has a number of drawbacks. Sequencing of transistor switching necessitates additional sensors with feedback on-line control. Particularly, as reported in references [7,9], the instants of turn-off transistor T_{r1} are difficult to control.

Other disadvantages concern continuous operation of the resonant circuit, which can deteriorate a modulation strategy. Moreover, the circuit is sensitive to the load current Io changes. Simulation example in Fig. 3 depicts an out of control capacitor overcurrent I_c, following the change of load current Io sign. Also the DC bus voltage transition rate dU_f/dt is significantly influenced by the difference between maximal inductor current and the load current ($I_{Lo} - I_o$).

In order to evaluate energetic efficiency of the considered circuits, we compare trajectories of reactive energy storage cycle for the positive load current I_o as in Fig. 3. The reactive energy transients have been represented in two dimensions, respectively to the inductive and capacitive components.

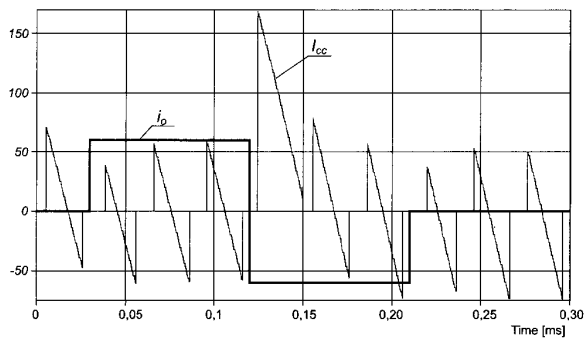

Fig. 3. ACRDCLI — simulation results; i_o — load current, I_{cc} — main capacitor current.

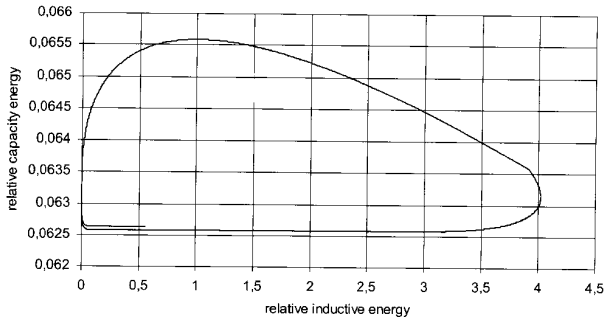

Fig. 4. ACRDCLI — trajectories of reactive energy storage in passive circuit components; (I_o = +60A)

Trajectories have been normalized with the reference to base reactive energy components, referred to the DC bus voltage U_{dc} and the load current I_o rating. The base capacity energy is carried by the main resonant capacitor C and auxiliary capacitor C_r,

$$E_{cb} = \frac{(C + C_r)U_{dc}^2}{2} \tag{1}$$

the base inductive energy is carried by the inductor L

$$E_{lb} = \frac{LI_o^2}{2} \tag{2}$$

Main energy flow is circulating in the inductor L.

The following modified active clamped QRDCLI scheme has been proposed by Salama et al. [14]. The main feature over precedent circuit is an execution of only one resonant cycle each time the switching state of the inverter has to be changed (Fig.5). During steady state the auxiliary and main capacitors C_1, C_2 are charged up to $kU_{dc} = UC_2$, where k is a factor between 1.2 – 1.5, [3]. The cycle is triggered at the instant t_0, when transistors T_1, T_2 are turned-on. Then inductor current decreases linearly

$$\frac{di_L}{dt} = \frac{U_{dc} - U_{C2}}{L} \tag{3}$$

At instant t_1, the transistor T_2 is turned-off. Negative inductor current i_L circulates through the U_{dc} source, capacitor C_1 and transistor T_1, quickly recharging small capacity of C_1. At t_2, the input inverter voltage U_f is decreased to zero, while the inductor current i_L, still negative, is commutated to the inverter free-wheel diode D_f. After resonant transition of the i_L to positive value, the inverter transistors T_f are short circuited. When the transistor T_f is switched-off, the positive i_L current charges again the capacitor C_1, rebuilding inverter input voltage U_f up the U_{C2} level. Then the main capacitor C_2 is charged by diode D_2 to the same value of U_{C2}. Since the inductor current i_L has reached zero, the resonant cycle is over and steady-state dc input voltage U_{dc} is passed to the inverter input.

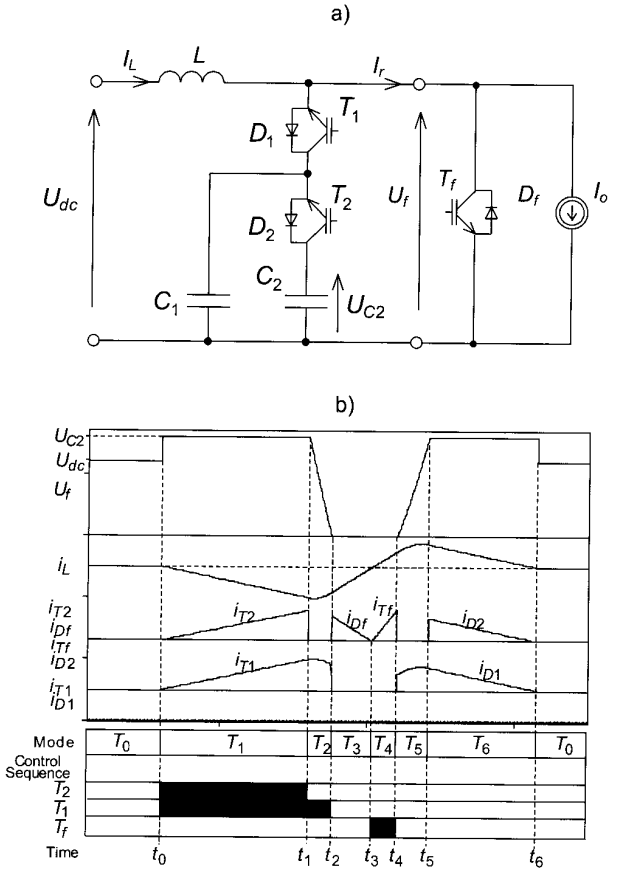

Fig. 5. Salama et al. circuit principles; a) scheme, b) waveforms and gating sequences

As in the previous scheme, to assure the operation, the main capacitor voltage U_{C2} must be controlled. Another precaution refers to limitation of charging capacitor C_2 current during initialisation process [3].

In normal conditions, the load current I_o is conducted by the inductor L (Fig. 6). At the commutation periods, inductor current i_L is resonantly oscillating due to the circuit operation cycle presented in Fig. 5. Input inverter voltage U_f, due to the U_{C2} spikes superimposed at the beginning and the end of resonant cycles, deteriorates modulation process. Resulting harmonic distortions may propagate to the output inverter voltage spectra. As has been tested by simulations,

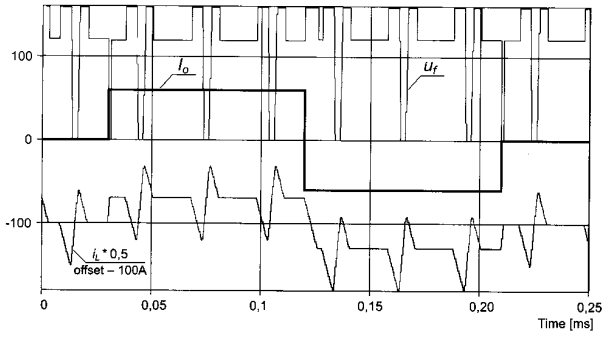

Fig. 6. Salama et al. circuit—simulation results; U_f—input inverter voltage, i_L—inductor current, I_o—load current

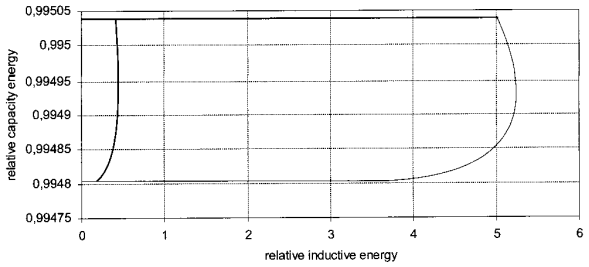

Fig. 7. Salama et al. circuit–trajectories of reactive energy storage in passive circuit components; (I_o = +60A)

the width of voltages spikes U_{C2} and of zero voltage periods are independent of load current I_o. However, the circuit is sensitive to the load current derivatives dI_o / dt. The positive transitions produce zero state voltage spikes due to inductor reaction, while the negative transitions, advantageously, are clamped by diodes–capacitor scheme arrangement.

The reactive energy trajectories in comparison to the Divan and Skibinski scheme indicate bigger portion of energy stored in the passive circuit components. The main part of capacity energy is stored in capacitor C_2, which is only partly recharged during resonance cycle. The inductor energy depends on the load current I_o direction.

2.2. Parallel quasi-resonant DC link inverter

The PQRDCLI inverter is characterized by parallel to the bridge inverter displacement of resonant intermediate circuit. One of the first schemes has been developed by Sul and Choi [5] (Fig. 8). At steady-state the load current I_o is conducted by the transistor T_1. Resonant cycle is started at the instant of switching-on transistor T_2. Then, auxiliary current starts to flow in the circuit form dc source U_{dc} through transistors $T_1 - T_2$ to capacitor C and inductor L. At the instant t_1, when transistor T_1 is turn-off the positive inductor current i_L is commutated to the circuit consisted of the auxiliary capacitor C_f, transistor T_2 and capacitor C. Due to small capacitance C_f, it follows quick recharging period and the voltage U_f decreases to zero at the instant t_2. The inductor L energy is then reloaded through the return diode D_f. Since inductor current i_L undergoes to negative value at the instant t_3, the inductor current i_L conduction is assured by the transistor T_f, capacitor C and diode D_2. At the instant t_4, when transistor T_4 is turned-off, the resonant process energy is transmitted to rebuild the voltage U_f across capacitor C_f. During this period, after recharging the main capacitor C at t_5, the inductor current i_L flows through the diode D_3. The voltage U_f across the C_f is approaching the input voltage U_{dc}, while exceeding inductor energy is returned to the voltage source U_{dc} by the diode D_1.

In long term simulation, at motor and generator I_o sequences, a stable operation of the resonance circuit is obtained (Fig. 9). The T_1, T_2 transistors switching mode is effected in a sensorless mode. Attained tolerance of passive elements is within the range of ±10%.

For stability of inductor current i_L cycling, particulary transistor T_f switch-on period must be precisely controlled.

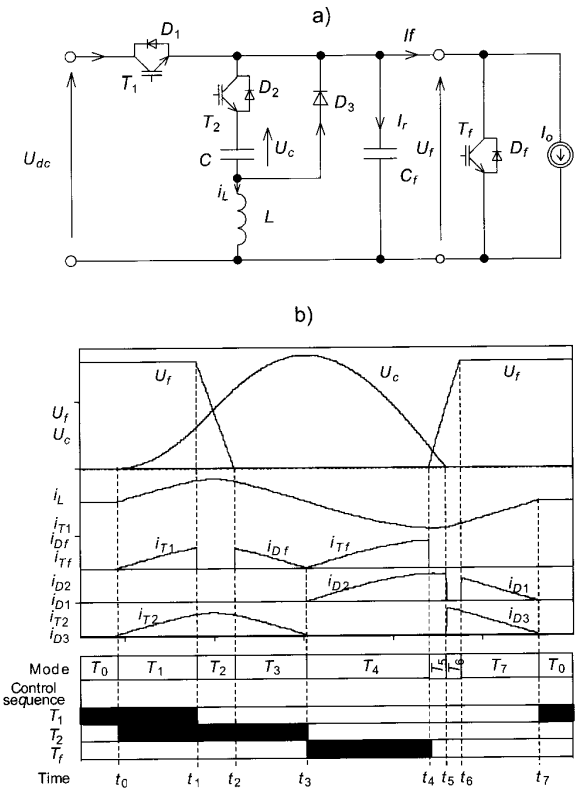

Fig. 8. Sul and Choi circuit principles; a) scheme, b) waveforms and gating sequences

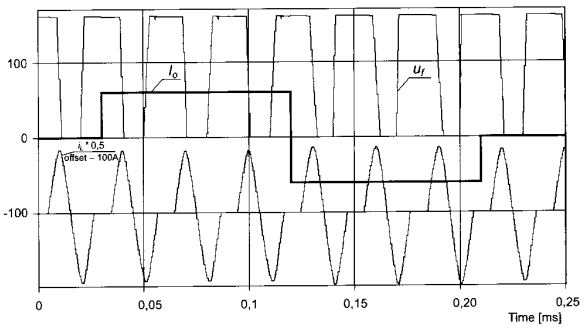

Fig. 9. Sul and Choi circuit—simulation results; U_f—input inverter voltage, i_L—inductor current, I_o—load current

Then, i_L current transitions without dc offset are assured. Resonant amplitudes are almost independent of load current. However, its values reach triple amplitude of load current I_o. Zero voltage link period, adjusted at 9μs, allow safe ZVS of inverter. This period is also not influenced by the load current I_o.

Trajectories of reactive energy are normalized to represent motoring (I_o = 60A) cycle. Significant part of reactive energy stored is of inductive type. Trajectories are robust to the load current I_o changes, indicating resonant character of energy exchange between inductor and capacitor LC tank.

The next circuit classified to the PQRDCLI inverters has been presented by Yoshitsugu et al. [15–16]. The operation cycle is similar to the precedent circuit. In order to initialise

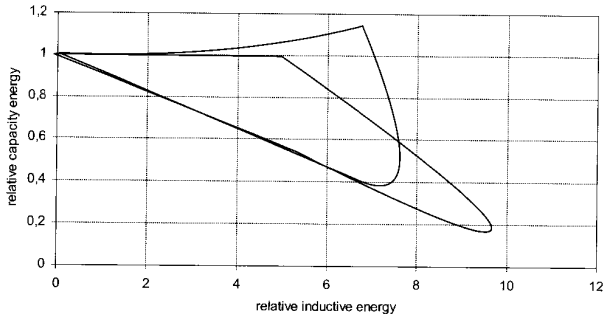

Fig. 10. Sul and Choi circuit—trajectories of reactive energy storage in passive circuit components; (I_o = +60A)

resonant mode, the transistors T_2, T_3 are turned-on at time instant t_0. Then, inductor current i_L linearly increases. At the instant t_1, transistors T_1 and T_3 are switched-off, commutating inductor current i_L to charge main capacitor C. The conducted circuit is closed by the auxiliary capacitor C_f and transistor T_2. At the instant t_2, the capacitor C_f is discharged, allowing zero link voltage state to switch the inverter. At that time, inductor current continuous to flow by the free-wheel inverter diode D_f. As inductor current i_L change the sign, it circulates through the inverter transistor T_f. When the inductor current i_L approaches negative amplitude at instant t_4, the transistor T_f is turned-off to enable recharge the auxi-

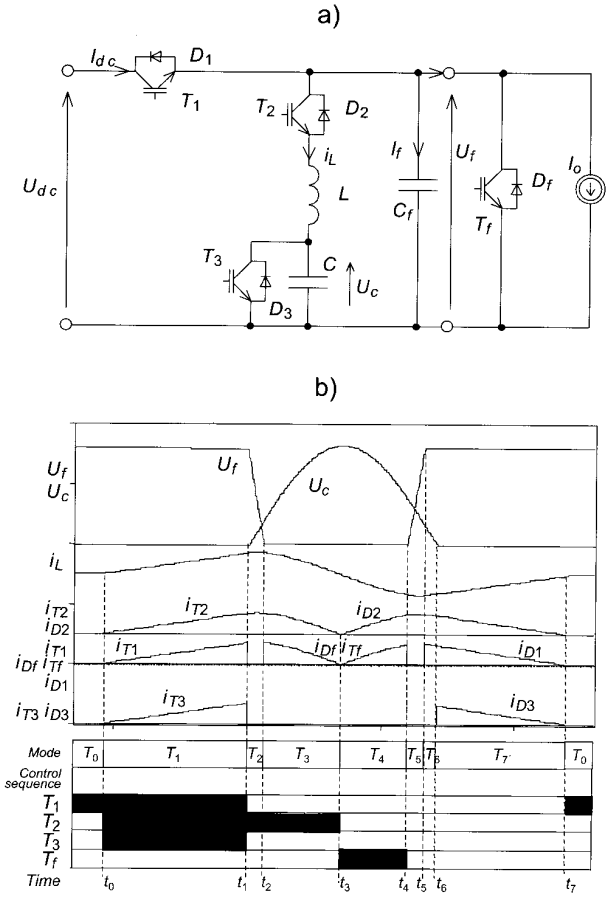

Fig. 11. Yoshitsugu et al. circuit principles; a) scheme, b) waveforms and gating sequences

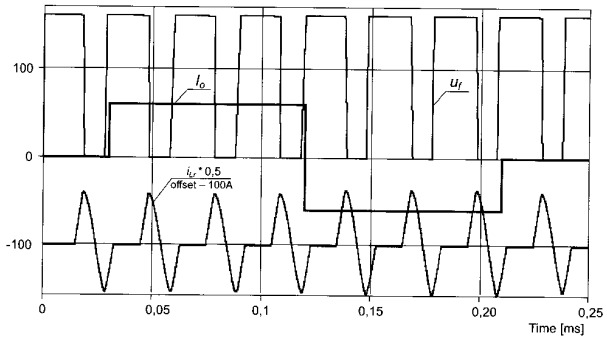

Fig. 12. Yoshitsugu et al. circuit—simulation results; U_f—input inverter voltage, i_{Lr}—inductor current, I_o—load current

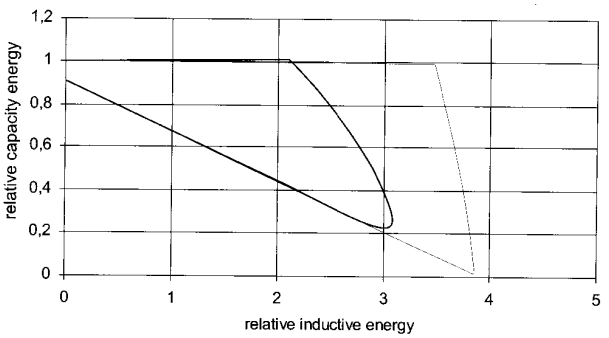

Fig. 13. Yoshitsugu et al. circuit—trajectories of reactive energy storage in passive circuit components; (I_o = +60A)

liary capacitor C_f and rebuild input inverter voltage U_f. At this time is conducted the diode D_1 to return to the source U_{dc} the excessive inductive energy. At the end of this process, at instant t_7 the transistor T_1 is turned-on to restart steady-state conditions.

Some circuit properties can be derived, from systematic simulation tests (Fig. 12). Application of the auxiliary transistor T_3, in comparison to the Sul circuit, profits a noticeable decrease of resonant inductor current i_L. The T_3 turn-off instant t_4 can be evaluated from load constraints and the reference of zero link voltage period (Fig. 11). Moreover, varying the turn-off instant t_4 one can influence the derivative of inverter voltage build-up dU_f/dt. A disadvantage of using transistor T_3 is its non-zero current switching-off process. In comparison to the Sul et al. circuit, transistors gating precision is more tolerant and energetic trajectories indicate lower energy storage requirements (Fig.13).

Another prototype of the PQRDCLI scheme has been recently proposed by Kurokawa et al. [12]. It can be characterized by an ability to control the zero link voltage interval without any conduction power loss. Circuit operation is described with connotation of Fig. 14.

At the instant t_0, transistor T_2 is turned-on, which begins linear increase of the inductor current i_L. Next, at certain i_L limit level corresponding to the instant t_1, transistor T_1 is turned off. Then, positive inductor current i_L increases resonantly and circulating through the capacitor C_f decreases link voltage U_f to zero at the instant t_2. At this moment, zero voltage turned-on of the transistor T_f takes place. Due to large time constant, still positive inductor current i_L circulates through diode D_f. At the instant t_3 when transistor T_2 is

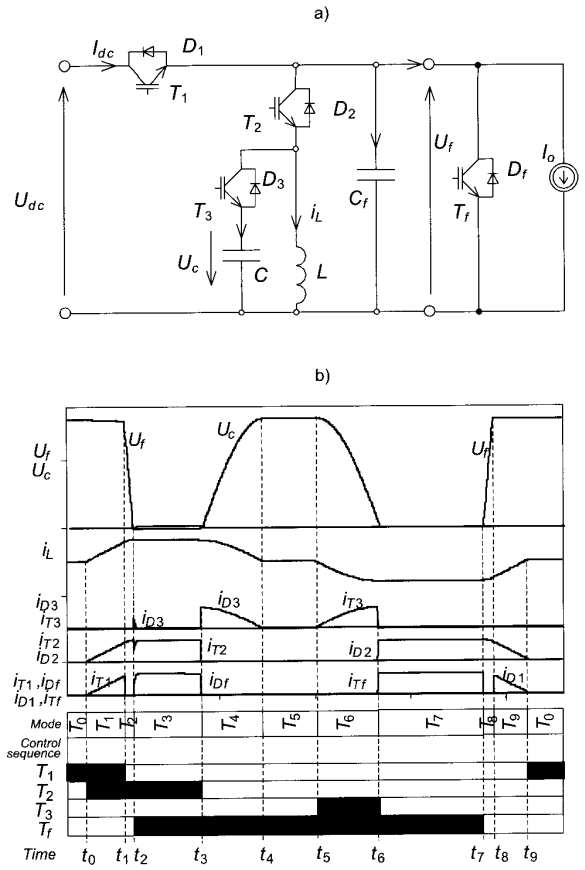

Fig. 14. Kurokawa et al. circuit principles; a) scheme, b) waveforms and gating sequences

turned-off, the capacitor C is charged resonantly to U_c, while inductor current i_L decreases to zero at the instant t_4. Then, components of the circuit can remain stable, until the transistor T_3 is turned-on. At that time resonant recharge of the capacitor C through the inductor L. At the instant t_6 of complete energy transfer from C to L, transistor T_3 is turned-off. Negative inductor current is conducted by the diode D_2 and transistor T_f. Switching-off the transistor T_f at the instant t_7 restarts recharging resonantly the auxiliary capacitor C_f to U_{dc}. An excess energy is transferred to the source by the diode D_1. The commutation cycle is over at the instant t_9.

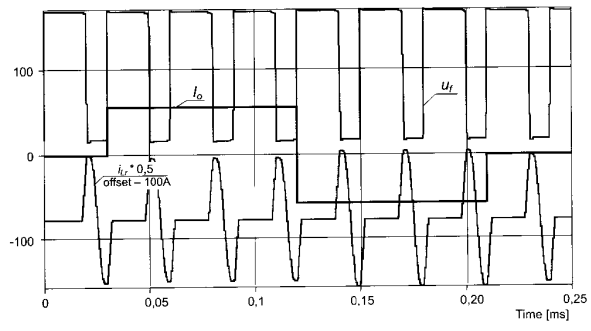

Fig. 15. Kurokawa et al. circuit—simulation results; U_f—input inverter voltage, i_{Lr}—inductor current, I_o—load current

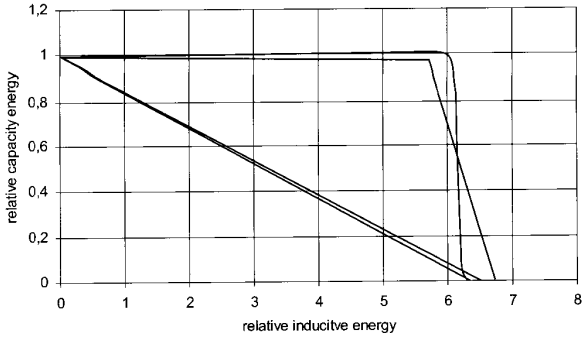

Fig. 16. Kurokawa et al. circuit—trajectories of reactive energy storage in passive circuit components; (I_o = +60A)

Despite the need of additional sensors U_f, U_c, i_L, in prototype circuit described by Kurokawa et al. [12], a dimensioning of passive elements, during simulation, has proved stable operation at positive sequence of load current I_o (Fig.15). The reactive energy trajectories, indicate regularity independent of load current direction (Fig.16). Maxima of inductive energy indicate significant more storage as compared to Yoshitsugu et al. [14] circuit operation conditions (Fig.13).

3. COMPARATIVE EVALUATION

One of the basic features of resonant dc voltage link inverters is ability to limit the rate of output voltage derivatives dU_f/d_t. In the following analysis obtained from simulation,

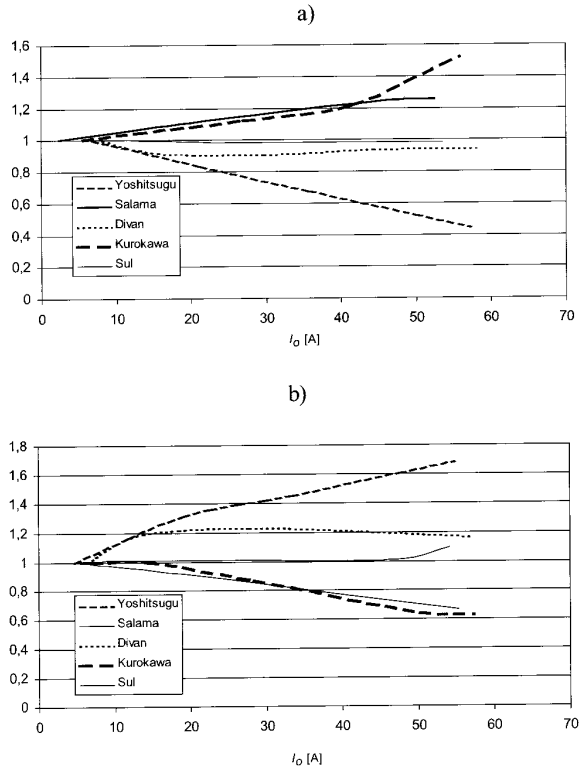

Fig. 17. Inverter voltage dU_f/dt sensitivity to the load current I_o changes; a) falling edge, b) raising edge

Table 1. The main features of structures

			Divan [8]	Salama [3,14]	Sul [5]	Yoshitsugu [14]	*Kurokawa* [12]
elements	T		1	2	2	3	3
	D		1	2	3	3	3
	L_C		3	3	3	3	3
switch operation conditions	*turn-off*	T_1	ZVS	ZVS, ZCS	ZVS, ZCS	ZVS, ZCS	ZVS, ZCS
		T_2	—	ZCS	ZCS	ZCS	HS
		T_3	—	—	—	ZVS, ZCS	—
	turn-on	T_1	ZVS	ZVS	ZVS	ZVS	ZVS
		T_2	—	ZVS	ZVS, ZCS	ZVS, ZCS	ZVS
		T_3	—	—	—	HS	ZVS
inverter input voltage			$1,2 \div 1,8 U_{dc}$	$1,2 \div 1,8\ U_{dc}$	U_{dc}	U_{dc}	U_{dc}
energy storage at steady-state			Yes	Yes	No	No	No
current stress of elements			$2\ I_o$	$2\ I_o$	$2\text{-}3\ I_o$	$2\ I_o$	$2\ I_o$
voltage stress of elements			$1,8\ U_{dc}$	$1,8\ U_{dc}$	U_{dc}	U_{dc}	U_{dc}

ZVS—Zero Voltage Switching,
ZCS—Zero Current Switching,
HS—Hard Switching

Table 2. Results of simulation and circuit data for loading current sequences $I_o = \pm 60A$, $U_{dc} = 160V$

Parameter		Divan [8]	Salama [3,14]	Sul [5]	Yoshitsugu [14]	Kurokawa [12]
peak inductor current [A]		+120/-134	+136/-161	+170/-190	+127/-112	+171/-167
main capacitor voltage [V]		40	160	183	169	176
zero link voltage period [μs]		4,9÷5,4	2,2÷2,3	8,8÷9,4	9,4÷9,55	6,1÷6,2
dUf/dt[V/μs] I_o {0÷60A}	fall	62÷77	207÷210	75÷95	220÷370	344÷520
	rise	62÷68	145÷159	52÷78	90÷210	188÷298
circuit data		C=470μF C_f=470nF L=7μH	C_1=470nF, C_2=2mF, L=2μH	C_f=2,2μF, C=6,2μF, L=4μH	C_f=470nF, C=3μF, L=5μH	C_f=470nF, C=2μF, L=2,2μH

are compared positive and negative voltage slopes as function of load current I_o changes. The respective derivatives are normalized to the values corresponding to zero load current for each of the considered circuit. In both cases, the best robustness manifests the Salama circuit, while the worse sensitivity depict the Yoshitsugu and Kurokawa schemes (Fig. 17).

In the Table 1, fundamental features of investigated circuits are to be compared using different criteria. The circuit complexity, which can be expressed by a number of circuit elements, is enhanced for a class of PQRDCLI schemes. Moreover, one of three transistors applied in circuits of Yoshitsugu [14] and Kurokawa [12] requires hard switching commutation. This is not the case of the Divan [8] and Salama [14] circuits. From the other side, additional voltage stress acting across active and passive elements of circuit is lower for PQRDCLI schemes. This feature is of great importance for medium and high voltage applications, where series component arrangement must be undertaken. Besides, the active clamped class of circuits with series inductor element opera-

te with nonzero inductive energy storage, which deteriorates their efficiency. All investigated circuits are characterized by at least double overcurrent stress related to the amplitude of the load current.

Despite the original circuits description requiring a number of on-line detectors or comparators, the simulation study has been developed in a sensorless mode. In the Table 2 are given characteristic data obtained for each of the investigated topologies, assuring stable simulated operation, independent of large transition sequences of the load current Io. Amplitudes of inductor current confirm circuits operation principles. The obtained zero link voltage periods possess margins for safe inverter state switching. However, significant zero voltage periods require compensation techniques for voltage modulation strategies. Voltage derivatives related to switching states have been drastically reduced as compared with hard commutation rates. The *LC* elements data are feasible, indicating lower values for PQRDCLI schemes.

4. CONCLUSION

In this paper different types of active clamped and parallel quasi resonant dc voltage link inverters have been compared in terms of circuit-oriented simulation. The operation of circuits was evaluated in time domain characteristics and reactive energy trajectories. In the particular example of load current motor-generator sequences, the successful resonant circuit operation has been obtained in a sensorless mode, without need of on-line voltage/current sensors or added comparators.

The most important common feature of evaluated RDCLI structures is a drastic reduction of voltage derivatives during transistor switching intervals, resulting from resonant soft-switching operation. Since the PWM inverter switching can be achieved in zero link voltage periods, the reduction of electromagnetic interference EMI is obtained without deterioration of overall efficiency of converter.

In response to a number of contradictory design objectives e.g.: circuit complexity, operation frequency, tolerance to gating accuracy, minimal energy storage or stress of passive components, various schemes have been recently developed. With the aid of simulation study, investigated resonant topologies have been particularly characterized, respectively to above criteria.

The technological progress of insulated gate bipolar transistors with expected increase of converter operation frequency indicates the advantages of RDCLI structures in range of medium power drive applications.

5. REFERENCES

1. Bachmann G.: *Resonant Switching on IGBT con-verters*, PCIM Europe 10/2000, pp. 34-36, 2000.
2. Bagawadi M., Fernande B., Subrahmanyam R.: *A novel quasi-resonant dc link inverter using cou-pled inductors*, EPE '99, Lausanne, 1999.
3. Bachmann G., Mutschler P.: *Comparison of PWM operated Resonant DC-Voltage Link Inverter*, EPE '99, Lausanne, 1999.
4. Chlebiś P.: *New concept of vector-modulated quasi-resonant dc link inverter*, 9th International Conference on Power Electronics and Motion Control, EPE-PEMC 2000 Košice, 2000.
5. Choi J.W., Sul S. K.: *Resonant Link Bidirectional Power Converter: Part I — Resonant Circuit*, IEEE Transactions on Industry Applications, pp. 479–484, 1995.
6. Cuzner R., Abel J., Luckjiff J., Wallace I.: *Evaluation of Actively Clamped Resonant Link Inverter for Low -Output Harmonic Distortion High-Power-Density Power Converters*, IEEE Trans. on Ind. Applications, pp. 847–855, 2001.
7. Divan D. M., Malesani L., Tenti P., Toigo V.: A *Synchronized DC Link Converter for Soft-Switched PWM*, IEEE Transactions on Ind. Applications, pp. 940–948, 1993.
8. Divan D. M., Skibinski G.: *Zero-Switching-Loss Inverters for High-Power Applications*, IEEE Transactions on Industry Applications, pp. 634–643, 1989.
9. Dzieniakowski M., Kanoza S.: *Parallel Resonant DC-Link Three Phase Inverter Analysis and Control*, Nowoczesne metody sterowania w energoelektronice i napędzie elektrycznym. P. Łódzka, Inst. Automatyki, Łódź, pp. 108–113, 1993.
10. He J., Mohan N., Wold B.: *Zero-Voltage-Switching PWM Inverter for High-Frequency DC-AC Power Conversion*, IEEE Transactions on In-dustry Applications, pp. 959–968, 1993.
11. Krogemann M., Clare J.C.: *A soft switching parallel Quasi Resonant DC-Link Inverter with Modified asynchronous space vector PWM*, Power Electronics and Variable Speed Drives, 23-25 September 1996, Conf. Publ. No.429, IEE, 1996.
12. Kurokawa M., Konishi Y., Nakaoka M.: *Evalua-tions of voltage-source soft-switching inverter with single auxiliary resonant snubber*, IEE Proc.-Electr. Power Appl. Vol.148, No.2 March 2001.
13. Malesani L., Tomasin P., Toigo V.: *Space Vector Control and Current Harmonics in Quasi-Resonant Soft-Switching PWM Conversion*, IEEE Transactions on Ind. Appl. pp. 269–277, 1996.
14. Salama, S.: *NovelSoft Switching Quasi Resonant 3-Phase IGBT Inverter*, EPE'95, Sevilla, pp. 2.095–2.099, 1995.
15. Yoshitsugu J., Ando M., Hiraki E., Inoue K., Nakaoka M.: *A Consideration on Soft Switching Inverter Using A Single Active Resonant Snubber for AC Motor Drive.* 9th Int. Conf. on Power Electr. Motion Control, EPE-PEMC Košice 2000.
16. Yoshitsugu J., Ando M., Hiraki E., Inoue K., Nakaoka M.: *Auxiliary Resonant DC Link-Assisted Soft Switching Inverter for AC Servo Motor Drive and Its Performance Evaluations*, EPE Graz 2001.

mgr inż. Sławomir Mandrek
received the M.Sc. degree in Power Electronics from Gdańsk University of Technology in 1994. From 1996 to 2002, he was with the Electrotechnical Institute — Gdańsk Branch. In 2002, he joined the Gdańsk Shiprepair Yard "Remontowa" S.A., presently working toward the Ph.D. degree in power electronics at the Gdańsk University of Technology, Poland. His research interests include power electronics, motion control, new topologies of power converters and computer simulation.

dr hab. inż. Piotr J. Chrzan, prof. PG
received the M.Sc., Ph.D., and Dr.Sc. degrees in 1978, 1988, and 1999, respectively, all from the Gdańsk University of Technology. Since 1980, he has been with the Faculty of Electrical and Control Engineering of the Gdańsk University of Technology. He is currently the Head of the Chair of Power Electronics and Electrical Machines. His research interests include modelling and control of electrical drives and power converters EMI optimisation. He is a member of the Editorial Committee of the Revue Internationale de Génie Electrique (Hermes-Lavoisier).