Estimation of Optimum Value of Y-Capacitor for Reducing Emi in Switch Mode Power Supplies

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Summary: Putting a Y-capacitor between the primary ground and secondary ground is a common practice in industry to reduce EMI; but, this capacitor increases touch current. A method is discussed to measure the touch current at circuit design level. An optimum value of Y-capacitor is predicted without exceeding touch current limit. Experimental results of touch current measurements and EMI measurements are analyzed.

Key Words:
EMI,
CM Noise,
Touch Current,
Y-capacitor

1. INTRODUCTION

Switching converter technology with isolation is used to design power supplies. It offers numerous advantages such as high efficiency, reduced transformer size and very good line regulation. But, it has drawbacks of low power factor and generation of Electromagnetic Interference (EMI). Various methods are available in literature for power factor improvement. All these methods use low order harmonic reduction, in turn transferring the energy to the higher end of the frequency spectrum, thus, further increasing the EMI problems. These interferences lie in the Radio Frequency Range; therefore, they are also called Radio Frequency Interference (RFI) [1].

Power semiconductor devices operating at high frequencies produce high frequency disturbances as an operational byproduct. All circuit components producing high rate of change of voltage and current are a potential source of EMI. The switching inverter is the major source of EMI in SMPS [1]. Some of the other parts responsible for generation and transmission of EMI are Parasitic Capacitances between PCB tracks, Parasitic Capacitances between collector (drain) and heat sink, Rectifier diodes, and various Inter-winding and Intra-winding capacitances of the SMPS transformer [2-6]. It is a good design practice to isolate and solve EMI problems at the initial design level itself. In industry, trial and error methods are often used to find the proper EMI suppression solutions.

It is an established practice in three wires SMPS to connect a capacitor between line and earth and also between neutral and earth terminals for EMI reduction. It provides a low impedance path to shunt the EMI current, thus preventing it to flow through LISN resistor [7]. This is called Y-capacitor. No such connection is possible in a two wire SMPS. Fortunately, the capacitor connected between primary and secondary return terminals of the power supply can serve as Y-capacitor to attenuate common mode (CM) noise [6,7]. Secondary ground is connected to earth either directly or through the parasitic capacitor between it and earth. Thus one terminal of Y-capacitor is always connected to earth. Another terminal of this capacitor is connected to Line and/or Neutral through high value bulk capacitor and rectifier diodes [7]. This method of connecting a capacitor between primary and secondary ground terminals has its own demerits. In most SMPS, transformer provides the isolation. Any capacitor connected like this increases touch current (leakage current) that flows across the primary and secondary isolation barrier when accessible parts are connected to the protective earth through a specified impedance value. Safety standards specify a limit for this leakage current to ensure human safety, preventing users from becoming part of a path for substantial current to earth when touching the output and/or the enclosure of a power supply. Therefore, a measurement of leakage current is required to be carried out to find out the maximum value of Y-capacitor which can be used to reduce EMI. In the present paper, a method is suggested to determine optimum value of Y-capacitor based on the maximum permissible value of leakage current. To visualize its effectiveness of EMI reduction, EMI measurement results are also presented.

2. LEAKAGE CURRENT MEASUREMENT

The method of leakage current measurement is shown in Figure 1 [8]. Mains voltage is applied to the unit under test (UUT). The current flowing between Line/neutral and any accessible part of the UUT through a 2K resistance (simulated resistance of the human body) is measured. This current should not exceed a value specified by the standards. For example, IEC60950 specifies a limit of 250μA for IT equipments [9].

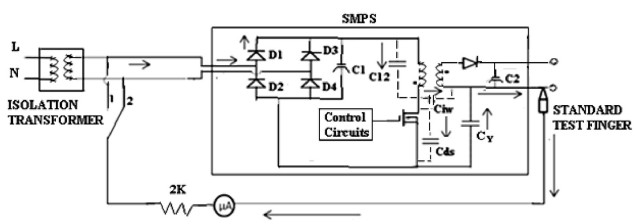

Fig.1. Method of Leakage Current Measurement

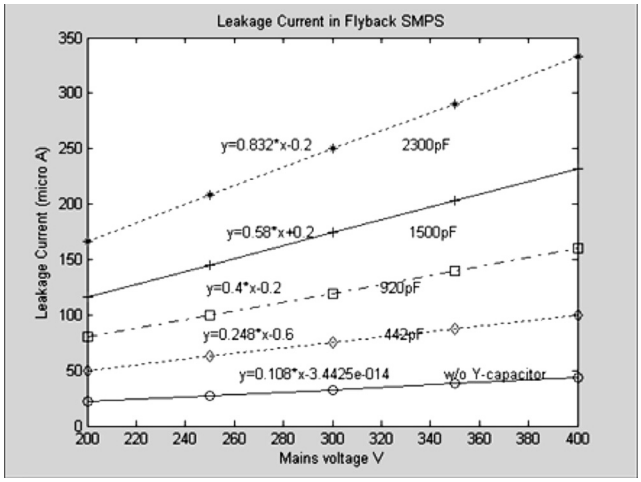

Fig. 2. Leakage Current in μA Vs Voltages for various values of C_Y in Fly-back SMPS

A 50W fly-back SMPS prototype was fabricated using UC3842 as the control IC for experimentation. Leakage current measurements were taken between Line and output terminal and then between Neutral and output terminal. First without a capacitor and then for various values of capacitors connected between primary and secondary return terminals of the transformer at various voltages. The voltage rating of the capacitors were selected high (3KV) as the insulation resistance of the transformer is tested at this voltage [8]. The tolerance of the capacitors used was ±5%.

Figure 2 shows the curves having linear relation between the mains voltage and leakage current, first when no Y-capacitor is connected and then for various values of capacitors (indicated in the graph) connected between primary and secondary terminals. The slope of each line is also given on it.

Since leakage current is contributed by the parasitic capacitances, the slope of the first straight line (w/o capacitor) gives the effective value of the inter-winding capacitances of the transformer. Using the linear curve corresponding to without capacitor, the value of inter-winding capacitor C_{iw} is obtained below:

$$\omega C_{iw} = 0.108*10^{-6}$$

or:

$$C_{iw} = 0.108*10^{-6}/2*\pi*f = 0.108*10^{-6}/314 = 343pF$$

The effective capacitor values are also calculated from other curves corresponding to different values of Y-capacitor connected, which are given in Table 1.

Table 1. Calculated and actual Values of Capacitor Combinations in Fly-back.

Calculated Values (pF)	Actual value of Parallel Combination (pF)
0.248*10-6/314 = 789	442+343 = 785
0.4*10-6/314 = 1273	920 + 343 = 1263
0.58*10-6/314 = 1847	1500 + 343 = 1843
0.832*10-6/314 = 2649	2300 + 343 = 2643

Thus, from the above calculations and discussion, we come to the conclusion that:

$$\text{Leakage Current} = \omega(C_Y + C_{iw})V$$

Therefore:

$$C_Y = (\text{Leakage Current}/\ \omega V) - C_{iw}$$

The effectiveness of Y-capacitor can also be seen from the following illustration:

The path for the leakage current is provided by the parasitic capacitors associated with the SMPS transformer. Figure 3 shows these capacitors for a fly-back transformer. Cds is the drain to source capacitor of the MOSFET switch. C_{12} and C_{34} are the intra-winding capacitors of the primary and secondary windings respectively. C_{13}, C_{14}, C_{23} and C_{24} are the inter-winding capacitors. Figure 4 shows various paths for the leakage current. The leakage current is measured between Line/Neutral and the output terminals. C2 is a large value filter capacitor connected at the output terminals which acts as a shot circuit at mains frequency. The parasitic capacitors provide various parallel paths between 1 & 4 for the leakage current to flow. One terminal of Y-capacitor is directly connected to 4 and another is connected to 1 through C_{12} & C_{ds}. Thus, Y-capacitor is seen to be connected in parallel to the current paths of parasitic capacitors, thereby, providing linear relation with the leakage current and the applied mains voltage between terminals 1 & 4.

The experimentation is repeated for a Half-Bridge Converter and the results are shown in Figure 5. The results are similar to the fly-back case and same conclusions may be drawn.

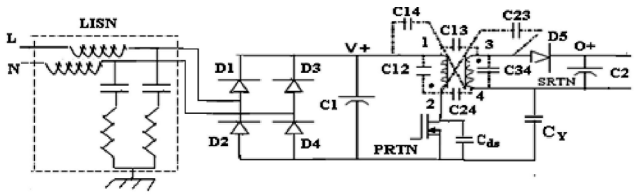

Fig. 3 The Fly-back SMPS and Parasitic Capacitors of the Transformer

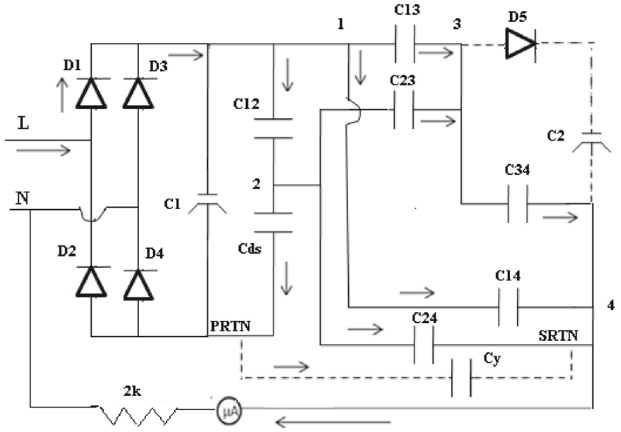

Fig. 4. Various paths for leakage current

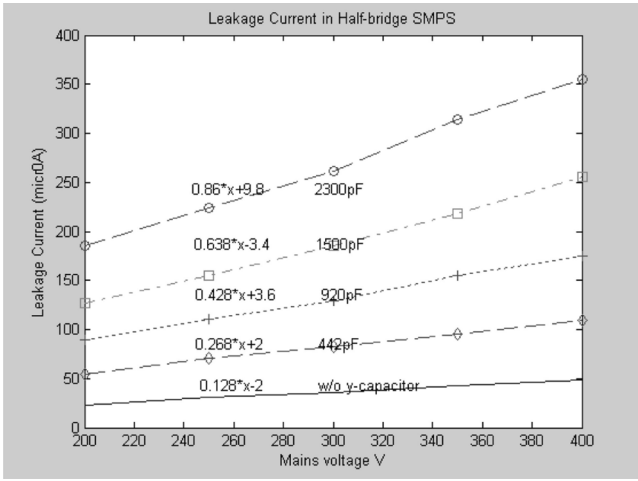

Fig. 5. Leakage Current in μA Vs Voltages for various C_Y values in a Half-Bridge SMPS

Using the linear curve corresponding to without capacitor, the value of inter-winding capacitor C_{iw} for this case is obtained below:

$$\omega C_{iw} = 0.128*10^{-6}$$

or:

$$C_{iw} = 0.128 *10^{-6}/2 * \pi * f = 0.128 *10^{-6}/314 = 407pF$$

The effective capacitor values are again calculated from other curves corresponding to different values of Y-capacitor connected, which are given in Table 2.

3. CONDUCTED MODE NOISE MEASUREMENT

For a leakage current of 250μA, the value of Y-capacitor at a voltage of 300V (worst case) for Fly-back prototype is calculated as:

$$C_Y = \{250\mu A/(300*314)\} - 350 = 2304pF$$

Table 2. Calculated and actual Values of Capacitor Combinations in Half-Bridge.

Calculated Values (pF)	Actual value of Parallel Combination (pF)
0.268*10-6/314 = 853	442+407 = 849
0.428*10-6/314 = 1363	920 + 407 = 1327
0.596*10-6/314 = 1898	1500 + 407 = 1907
0.860*10-6/314 = 2738	2300 + 407 = 2707

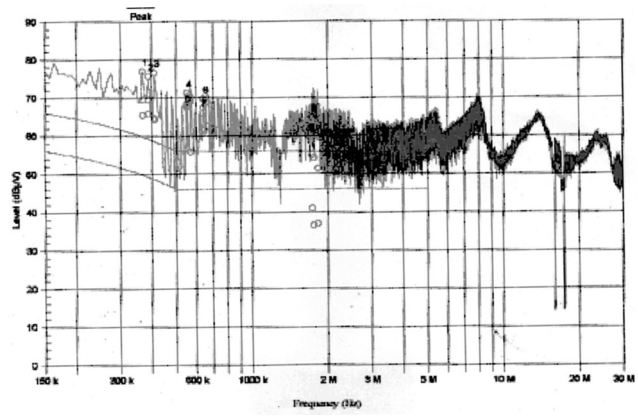

Fig. 6. Conducted Emission Measurement without any extra Capacitor

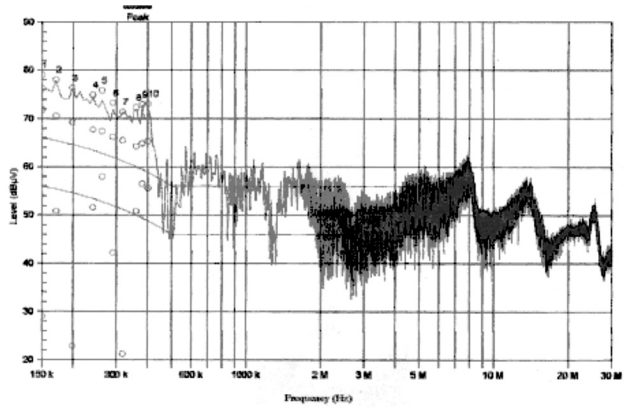

Fig. 7. Conducted Emission Measurement after adding a 920pF/3KV Y-capacitor between primary and secondary grounds

The Y-capacitor bypasses the noise current and prevents it from going to LISN. Increasing its value reduces EMI. To verify this effect, the conducted mode noise at the mains port of the Fly-back SMPS prototype was measured at ERTL (N), New Delhi, initially without any external capacitor and then with two capacitors (920pF and 2300pF) connected between primary and secondary return terminals. The measurements were carried out as per CISPR22© IEC 2003 [10]. Table 3 specifies the limits for conducted disturbance at the mains port of class B Information Technology equipment (ITE). The limits for Quasi peak and Average are also indicated in the graphs.

Figure 6 shows the CM noise measurements without connecting any Y-capacitor. All the peaks at various frequencies are well above the specified limits. Figure 7 shows the results after connecting a 920pF/3KV Y-capacitor between primary and secondary return terminals. Noise components between 0.15 MHz to 2.5 MHz does not pass the limits set by the standards. Components between 2.5 MHz to 4.5 MHz pass and then again all the components in the range of 5MHz to 30 MHz pass the limits. Figure 8 is the result with 2300pF/3KV Y-capacitor connected between primary and secondary return terminals. There is a marked reduction in EMI. All noise peaks from 2 MHz onwards are under specified limits.

Table 3:- Limits for conducted disturbances at the mains ports of class B ITE

Frequency range MHz	Limits dB(μV)	
	Quasi-peak	Average
0.15 to 0.50	66 to 56	56 to 46
0.50 to 5	56	46
5 to 30	60	50

Note 1: The lower limit shall apply at the transient frequencies
Note 2: The limit decreases linearly with the logarithm of the frequency in the range 0.15 to 0.50 MHz

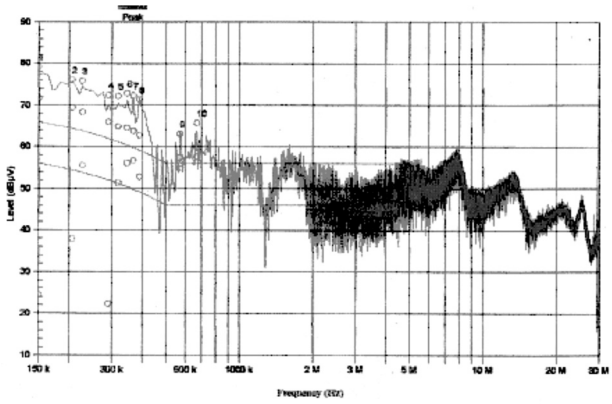

Fig. 8. Conducted Emission Measurement after adding a 2300pF/3KV Y-capacitor between primary and secondary grounds

Thus it is clear that the maximum value of capacitor which satisfies the leakage current limits at a worst case voltage (300V) is sufficient to reduce the EMI to reasonable limits. If the operation is performed at a lesser voltage than the value of this capacitor may further be reduced.

4. CONCLUSIONS

Connecting a Y-capacitor is useful to reduce EMI in higher end of the frequency spectrum. It returns the noise current back to the driving source. It is experimentally observed that by increasing the value of Y-capacitor the leakage current rises linearly while EMI reduces. It happens because the Y-capacitor shunts most of the EMI current. An expression for calculating the value of Y-capacitor is obtained by knowing the value of the leakage current. The proposed method is suitable to determine the highest value of Y-capacitor to be used to provide the maximum EMI reduction by knowing upper limit of the permissible leakage current.

5. ACKNOWLEDGEMENTS

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