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Application of Z-Source Converter in Photovoltaic Grid-Connected Transformer-Less Inverter

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Summary: **In PV grid connected power conditioners, usually both stepping-up the PV array voltage, and stepping-down the dc bus voltage for injection of a sinusoidal current to the grid is required. In this paper the design procedure of Z-source converter as a single phase PV grid connected transformer-less inverter is presented. The converter has one switch less than the conventional two stage power conditioner, which leads to reduction of cost. An optimum modulation pattern for the switches is proposed, and the low frequency ripple of the converter is modeled. The design of the converter is verified by simulation.**

Key words:
photovoltaic power conditioner (PV PCU), grid-connected systems, Z-source inverter, inverter

1. INTRODUCTION

In recent years, the photovoltaic (PV) grid connected systems become more popular [1]. A Power Conditioner Unit (PCU) links the PV arrays to the gird. The PV-PCU converts the DC power produced by PV-arrays to AC power, compatible with grid standards. In 220V networks the PV-PCU boosts the level of PV-arrays output to generate proper voltage level and supplies the network with AC current. Usually PV-PCU consists of a boost converter and a current controlled voltage source inverter (VSI) [2]. Also some single stage inverters with boosting ability have been suggested [3, 4].

Many PV-PCUs use a low frequency isolation transformer. To use of the high frequency isolation transformer, reduces the weight and increases the efficiency of converter [5]. Newly developed standards allow transformer-less topologies [6].

Reduction of the component cost is a target of research in PV grid connected systems. Omission of the isolation transformer, and use of a single-stage modified boost inverter, helps the development of a cost-effective PV-PCU.

An impedance-source inverter for three phase loads such as ac motors, supplied by fuel cell, has been presented in [4]. It can be used for a single-phase PV-PCU as Figure 1. The modulation method and design procedure of it is presented in the following sections.

2. Z-SOURCE CONVERTER MODULATION

The boost function is achieved by opening and closing the full bridge switches. There are different modulation methods. It is possible to short the bridge by closing alternative legs (Q1, Q3 or Q2, Q4) or by all four switches. Also opening the bridge can be done by turning off upper or lower switches (Q1, Q2 or Q3, Q4) or by all four switches.

Both unipolar and bipolar modulation is possible for inverter section. Unipolar technique is preferred, since it produces fewer harmonic compared with bipolar method [7]. For the Z-source inverter, the unipolar technique permits higher modulation index with lower dc bus voltage. The optimum switching pattern is proposed as Figure 2.

In this Pattern the upper switches (Q1, Q2) are turned on, alternatively, with the frequency of f_o where f_o is the output frequency of inverter. The lower switches are driven with the switching frequency of the converter. Their duty cycles are different in subsequent half periods of the output waveform. When Q1 is on, Q3 should provide the boost function, therefore, its duty cycle is controlled to maintain the required dc bus voltage. Synchronously, Q4 generates the SPWM, and its duty cycle is determined by the required modulation index.

The SPWM command is always given at the beginning of the switching period, and the end part of the switching period is specified for the boost duty cycle (Fig. 3). Freewheeling of the inverter (provided by D2 when Q1 is on) starts after SPWM command and extends to the end of the switching period.

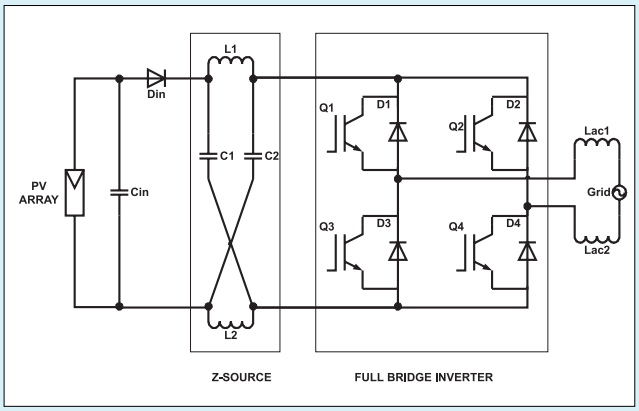

Fig. 1. Z-source inverter topology

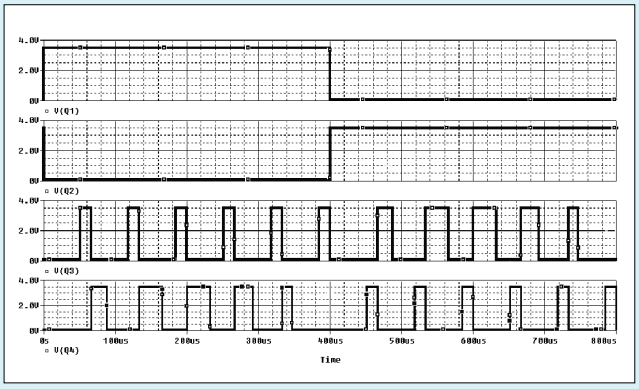

Fig. 2. Proposed switching pattern for the Z-source inverter for m = 0.5 and f_s/f_o = 12.

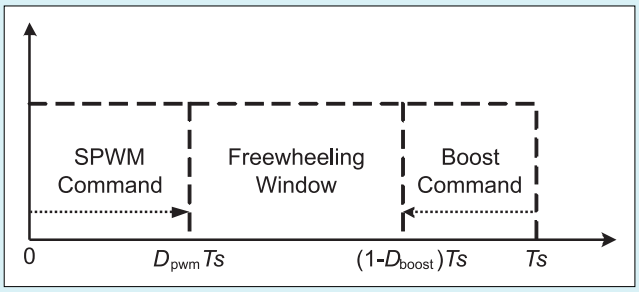

Fig. 3. Partitioning of the switching period

The proposed method has the following advantages:

1. The boost interval is also used for freewheeling of inverter and permits higher modulation index.
2. The common mode EMI is low [8].
3. Q1 and Q2 have low frequency switching loss.
4. There is ZVS for Q4 or Q3 alternatively.
5. The proposed method provides lower switching loss, which is dominant for IGBTs used at high switching frequencies.

To distribute the switching loss more evenly, the switching pattern can be changed alternatively, between the upper and lower IGBTs.

3. CONVERTER DESIGN

The boost performance of the Z-source converter has been investigated in [4]. The dc bus voltage is expressed as follows:

$$\frac{V_{dc}}{V_{in}} = \frac{1}{1-2D_{boost}} \tag{1}$$

where:

V_{in} — is the input voltage,

V_{dc} — is the dc bus voltage across the bridge, when it is not short,

D_{boost} — is the duty cycle of shoot through time interval.

The voltage of capacitor C_1 (and C_2) is related to the input voltage as (2):

$$\frac{V_{C_1}}{V_{in}} = \frac{1-D_{boost}}{1-2D_{boost}} \tag{2}$$

The design procedure of the Z-source converter as a PV grid-connected power conditioner is given as follows.

The required dc bus voltage is determined by the maximum grid voltage:

$$m_{max}V_{dc} \geq \sqrt{2}V_{ac(max)} \tag{3}$$

where m_{max} is the maximum modulation index of the full bridge inverter, and it is related to the switching pattern of Figure 3 as (4):

$$m_{max} = D_{PWM(max)} = \frac{T_{PWM(max)}}{T_s} \tag{4}$$

m_{max} is limited by the minimum PV array voltage:

$$m_{max} \leq 1 - D_{boost(max)} \tag{5}$$

$D_{boost(max)}$ is determined by the minimum PV array voltage:

$$\frac{V_{dc}}{V_{PV(min)}} = \frac{1}{1-2D_{boost(max)}} \tag{6}$$

Combining (3), (5) and (6) result in:

$$D_{boost(max)} \geq \frac{\sqrt{2}V_{ac(max)} - V_{PV(min)}}{2\sqrt{2}V_{ac(max)} - V_{PV(min)}} \tag{7}$$

The output ac filter inductors should provide the required total harmonic distortion limit of the output current. They can be calculated according to (8) [8]:

$$I'_{L_{ac}(rms)} = \frac{V_{dc}}{2f_sL_{ac}}\frac{1}{2\sqrt{3}}\sqrt{\frac{1}{2}m^2 - \frac{8}{3\pi}m^3 + \frac{3}{8}m^4} \tag{8}$$

$$THD = \frac{I'_{L_{ac}(rms)}}{I_{L_{ac}(1)(rms)}} \times 100 \leq THD_{(req)} \tag{9}$$

Where, $I_{Lac(1)}$ is the fundamental frequency component of the output current, and $I'_{Lac(1)}$ is its ripple, and m is the modulation index. The maximum value of $I_{Lac(1)}$ is derived from (10):

$$I_{L_{ac}(1)} = \frac{P_{ac(max)}}{V_{ac(min)}} \tag{10}$$

(8) through (10) provide necessary data for design of L_{ac}. More detailed information can be derived from the simulation results.

The ripple current of input inductors is obtained from (11):

$$\Delta I_{L_1} = \frac{D_{boost}V_{C_1}}{f_sL_1} = \frac{D_{boost}(1-D_{boost})V_{dc}}{f_sL_1} \tag{11}$$

The total average current of L_1 for a dc load is:

$$I_{L_1(avg)} = \frac{P_{ac}}{\eta V_{PV}} \tag{12}$$

It is deducted from simplified circuit diagram of Figure 4, for a dc load.

Integrating the input current over a switching period results in:

$$I_{in(avg)} = I_{L_1(avg)} + I_{C_1(avg)} \tag{13}$$

For dc load $I_{C1(avg)}$=0. Multiplying both sides by V_{pv} results in:

$$P_{in} = I_{L_1(avg)} V_{PV} \tag{14}$$

Since $P_{in} = P_{ac} / \eta$, where η is the efficiency of the converter, then (12) is proved.

The capacitor C_1 energizes L_1 in shoot through interval. Its high frequency ripple for dc load is given by:

$$\Delta V_{C1} = \frac{D_{boost} I_{L_1}}{f_s C_1} \tag{15}$$

The electrolytic energy capacitors can be selected according to their rms ripple current and the excepted life time. Their nominal rms ripple current should be higher than the maximum capacitor ripple current at worst case operating condition.

For the dc load the rms ripple current of C_1 is derived in (16). It can be used for selection of C_1 and C_2.

$$I^2_{c_1(rms)} \approx D_{boost} I^2_{L_1} + D_{PWM} \left(I_{L_1} - I_o\right)^2 + \\ + (1 - D_{PWM} - D_{boost}) I^2_{L_1} \tag{16}$$

In a single phase inverter, the instantaneous output power is not constant and oscillates with the frequency of $2\omega_o$. This low frequency ripple should take into account for design of Z-source components, which is investigated in the next section.

4. LOW FREQUENCY RIPPLE CONSIDERATION

The instantaneous output power, for a unity power factor inverter expressed as follows:

$$p_o = P_{ac}(1 - cos 2\omega_o t) \tag{17}$$

The first term is the active power, which is used in (12) to calculate the dc component of I_{L1}. The second term causes a $2\omega_o$ ripple in the current and voltages of Z-source elements. An approximate analysis is given here for consideration of this effect.

During non shoot through interval, energy is transferred from dc bus of full bridge converter to the grid. The instantaneous input power to full bridge converter in Figure 4 can be expressed as:

$$p_{fb} = V_{dc} \bar{i}_{fb} \tag{18}$$

$\bar{I}_{fb}$ is the full bridge current, in non shoot through interval, averaged over T_s. If we assume that output inductors (L_{ac}) do not store too much energy, the input instantaneous power of the full bridge should be equal to the output instantaneous power delivered to grid. Considering the efficiency of the converter:

$$p_{fb} \approx \frac{p_o}{\eta} \Rightarrow \bar{i}_{fb} \approx \frac{P_{ac}}{\eta V_{dc}} (1 - cos 2\omega_o t) \tag{19}$$

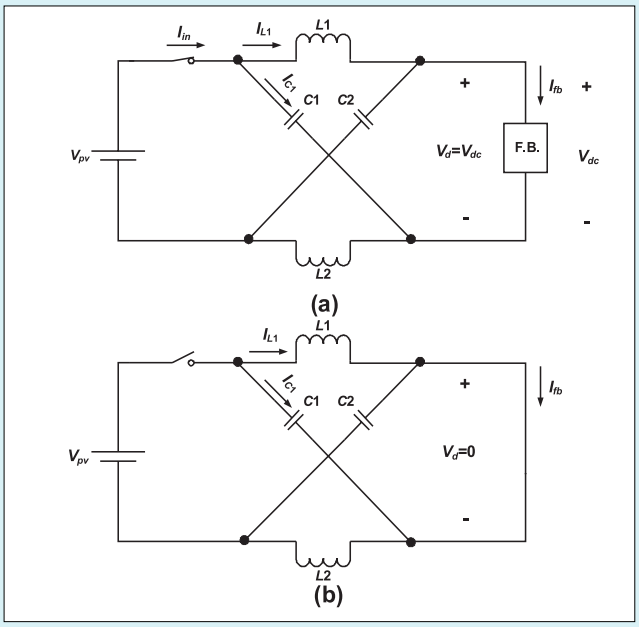

Fig. 4. Simplified circuit diagram of the converter during, (a) non shoot through interval and (b) shoot through interval

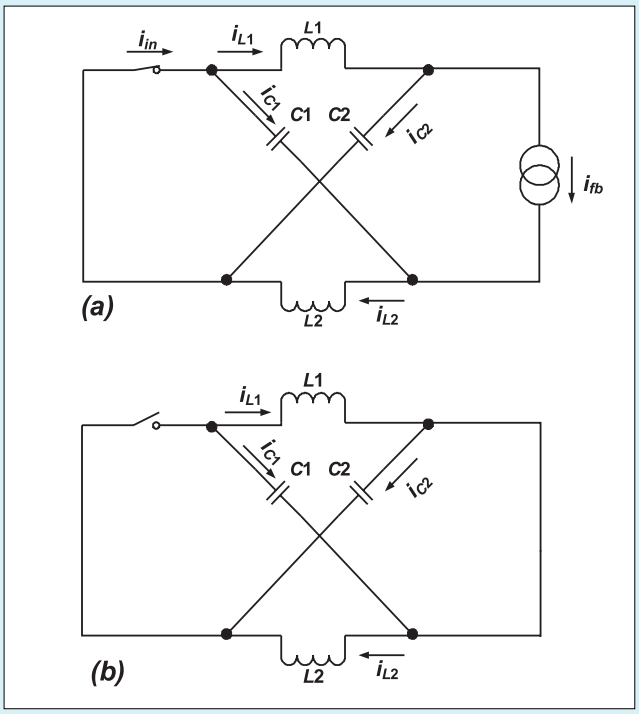

Fig. 5. Equivalent circuit for deriving the low frequency ripples

The low frequency component of $\bar{I}_{fb}$ is denoted by $\tilde{i}_{fb}$ which is given by (20):

$$\tilde{i}_{fb} \approx \frac{P_{ac}}{\eta V_{dc}} cos 2\omega_o t \tag{20}$$

It is modeled as a current source in Figure 5a to calculate the low frequency ripple of Z-source elements. Determining how it is divided between the inductors and capacitors is a difficult task. Because $\bar{I}_{fb}$ acts as slow varying current source for consequent switching cycles, and both time varying initial conditions and transients should be considered. A simple approximate solution can be given as follows:

Table 1. Power conditioner specifications

$V_{PV(\min)}$	180V
$V_{PV(\max)}$	450V
$P_{in(\max)}$	1800W
THD	<5%
$V_{ac(\max)}$	235V
$V_{ac(\min)}$	195V

Table 2. Design parameters of the converter

D_{boost}	0.227	L_{ac}	3.8mH
m	0.591	ΔI_{L1}	2.4A
f_s	15KHz	L_1	2.7mH
THD	4%	C_1^*	340μF
I'_{Lac}	0.3A		

For operating point of V_{PV} = 300V, V_{ac} = 230V, P_{ac} = 1750W
* Two 680μF in series

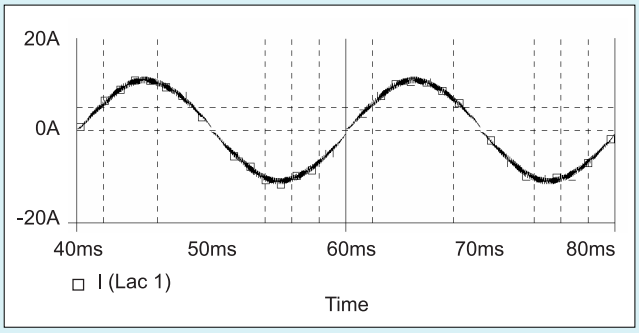

Fig. 6. Output current at P_{out} = 1750W

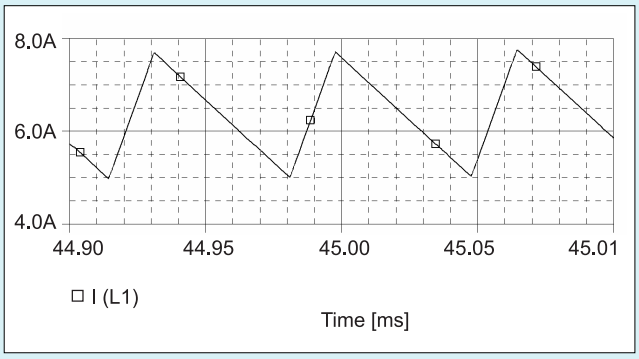

Fig. 7. High frequency ripple of L_1 current

At the switching frequency of f_s the impedance of inductors are much higher than the impedance of the capacitors, therefore, we assume that $\bar{I}_{fb}$ passes completely through the capacitors:

$$\tilde{i}_{C_1} = -\tilde{i}_{fb} = -\frac{P_{ac}}{\eta V_{dc}} cos2\omega_o t \qquad (21)$$

The low frequency ripple current develops a low frequency ripple voltage in the capacitors:

$$\tilde{v}_{C_1} = \frac{1}{2\omega_o C_1}\tilde{i}_{C_1} \qquad (22)$$

Since in shoot through interval, the capacitors are in parallel with the inductors (Fig. 5b), their low frequency voltage ripple leads to a low frequency current ripple in the inductors.

5. VERIFICATION OF DESIGN PROCEDURE

In this section the proposed method is verified by a design example. The design requirements of the PV-PCU are given in Table 1. Using (6) and (7), $D_{boost(\max)}$ and V_{dc} is derived as follows: $D_{boost(\max)}$ = 0.332 and V_{dc} = 535V.

V_{dc} = 550V is chosen. The design is followed for the V_{pv} = 300V and V_{ac} = 230V, which is considered as the nominal input and output voltage of the converter, respectively. The design parameters, using the procedure of section III and IV are presented in Table 2.

The converter with the parameters of Table 2 has been simulated by PSpice. Figure 6 shows the output current of the converter. THD is about 4.5%. Figure 7 shows the high frequency ripple current of L1. ΔI is 2.7A at the time instant which has been shown in the Figure.

The current and voltage waveforms of the switches Q1, Q4, Q3 and the diode D2 are shown in Figure 8. They belong to the positive output sinusoidal half cycle. As can be seen, Q1 has not high frequency switching loss, and ZVS for Q4 has been provided.

The current delivered to the bridge, at non shoot through intervals, averaged over one period of switching, is shown in Figure 9. The waveform resembles (1–cos2$\omega_o t$) function, as predicted by (19).

To prove that this low frequency ripple current goes almost through the capacitors C_1 and C_2, the waveform of the locally averaged C_1 current is presented in Figure 10. The amplitude is 3.14 A which is very close to 3.2A, predicted by (21). Figure 11 shows the low frequency ripple of C_1 voltage which is 30.67V peak to peak. According to (22) it is 30.6Vpp.

The simulation was repeated with $C_1 = C_2$ = 680μF. The results show that the locally averaged capacitor currents are almost the same as before, but their low frequency voltage ripples are divided by two.

The prototype of the PV-PCU is under construction, and will be reported in future.

VI. CONCLUSION

The design procedure of the Z-source converter as a single phase PV grid connected transformer-less inverter has been presented in this paper.

An optimal switching pattern for the modulation of the converter has been proposed, which reduces the switching loss and common mode EMI. In single phase application, the output power is not constant and leads to a low frequency ripple in the converter elements. An approximate analysis has been proposed, which considers this effect. The validity of the design method has been verified by simulation.

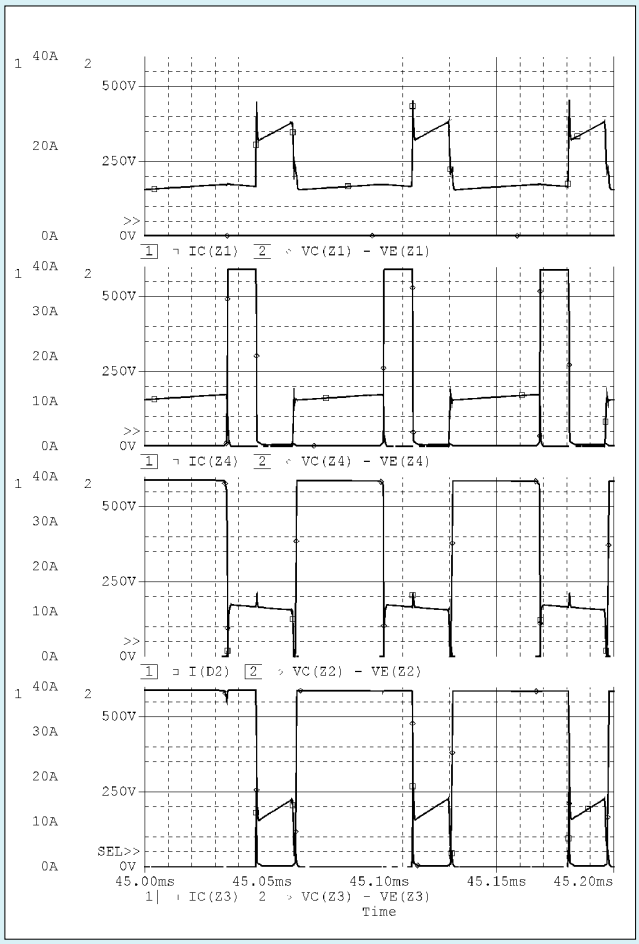

Fig. 8. Current and voltage waveforms of the switches Q1, Q4, Q3 and the diode D2

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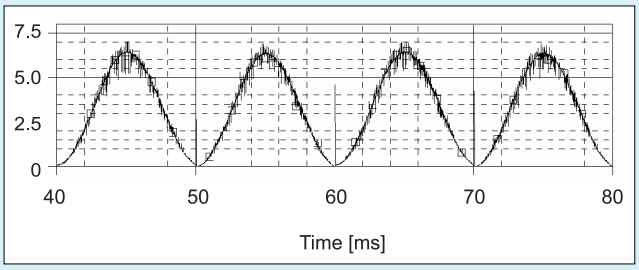

Fig. 9. Current delivered to the bridge, at non shoot through intervals, averaged over one period of switching

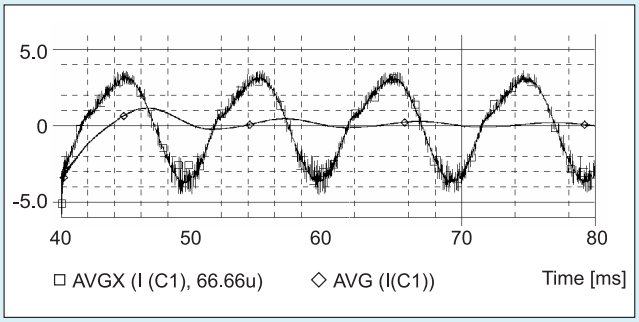

Fig. 10. Locally averaged current waveform of C_1

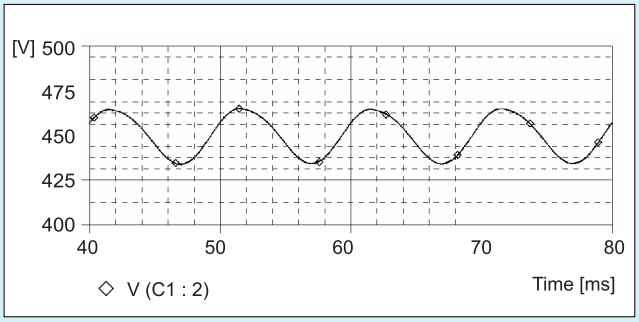

Fig. 11. Low frequency voltage ripple of C_1

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