

# Multiresonant ZVS CUK Converter

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**Summary:** The article presents properties of multiresonant ZVS Cuk converter. The control system of the converter is based on PWM technique. The operating range of the converter is defined where ZVS operation is assured. Control characteristics are given and the converter's efficiency is defined. The converter's operation is analysed on the basis of simulation testing.

**Key words:**

multiresonant converter, Cuk circuit, zero voltage switching (ZVS), resonant circuits

## 1. INTRODUCTION

Demand for resonant circuits converting DC/DC electricity switched at high operating frequencies is a result of attempts at great efficiency, minimizing size, and the consequent cost reduction of converters. Energy efficiency of high-frequency converters depends mainly on switching processes of semiconductor components. At turn-on and turn-off, power losses occur which are a result of current multiplied by voltage in switched semiconductor elements. At high operating frequency, parasitic inductances of connections and parasitic capacitances of transistors and diodes produce resonant circuits which generate parasitic electromagnetic oscillations. When the transistor is conducting, impact of rectifying diode's parasitic capacitance occurs, and when the reverse diode is conducting, the transistor's parasitic capacitance affects the circuit operation. Topologies of multiresonant converters (MRCs) enable application of switching technique at zero voltage of both the transistor and the diode. Switching of transistor and diode at zero voltage (ZVS) in MRCs allows for obtaining high operating frequency of the circuit while maintaining great energy efficiency and minimizing voltage and current oscillations.

References present basic topologies of ZVS MRCs and their characteristics [1, 3, 7, 11]. Properties of ZVS Buck MRC are analysed in [1, 10, 11]. Results of simulation testing for topologies of Boost and Buck-Boost ZVS MRCs are presented in references [5, 6].

This article concentrates on ZVS Cuk MRC topology. An analysis of the circuit's operation is presented based on results of simulation testing employing Simpler software.

## 2. TOPOLOGY OF ZVS CUK MRC

The structure of ZVS Cuk MRC is shown in Figure 1. High-inductance reactor  $L_F$ , in series with DC voltage  $E$ , provides constant current  $I_{LF}$  to the converter. Reactor at inductance  $L_{F1}$ , equal to inductance  $L_F$ , enforces constant current  $I_{LF1}$  to: capacitor at capacitance  $C_F$  and load resistance  $R$  in parallel connection. MOSFET  $T$  at resistance  $R_T$  when conducting and output capacitance  $C_{OS}$  is switched at frequency  $f$ . Diode  $D_S$  is an integral part of the transistor and enables bi-directional conducting of current  $i_S$ . The rectifying diode  $D$  includes a junction capacitance  $C_{OD}$ .

The converter's resonant circuit includes: reactor at inductance  $L$ , capacitor at  $C_S$  in parallel with the transistor  $T$

and capacitor at  $C_D$  in parallel with diode  $D$ . Capacitances  $C_S$  and  $C_D$ , in parallel with parasitic capacitances  $C_{OS}$ ,  $C_{OD}$ , build equivalent resonant capacitances of the circuit. Inductance  $L$  comprises parasitic inductances of the circuit. A very high quality factor of the reactor  $L$  is assumed, thus, the impact of reactor's resistance is ignored. The capacitor at  $C_F$  is a low-pass filter that limits ripples of output voltage.  $C_T$  is a large energy-transfer capacitor. The circuit in Figure 1, when PWM control is employed, enables ZVS of transistor  $T$  and diode  $D$ .

## 3. OPERATION OF THE CIRCUIT

In the Cuk MRC (Fig. 1), operating cycle is divided into five time intervals. Current and voltage waveforms during a cycle (relative units) based on simulation testing are shown in Figure 2. Resonant circuits for five time intervals of operation are presented in Figure 3.

In the first time interval ( $t_0 \leq t \leq t_1$ ) (Fig. 2), at  $t=t_0$ , transistor  $T$  is turned on. Voltages: drain — source transistor  $u_{CS}$  and diode  $u_{CD}$  equal zero. In the node 1 (Fig.3a), the value of  $i_L$  is greater than the supply current  $I_{LF} = \text{const}$ . The MOSFET's body diode  $D_S$  conducts difference  $i_L - I_{LF}$  in the circuit:  $D_S$ ,  $L$ ,  $C_T$ ,  $D$ . At  $t=t_1$ , the current  $i_L = I_{LF}$  and  $D_S$  stops conducting. The circuit in Figure 3a is described:

$$\begin{aligned} I_{LF} - i_S - i_L &= 0 \\ i_L - I_{LF1} - i_D &= 0 \\ L \frac{di_L}{dt} + u_{CT} + u_D + u_{DS} &= 0 \\ i_L &= C_T \frac{du_{CT}}{dt} \\ I_{LF1} - C_F \frac{dU_O}{dt} - \frac{U_O}{R} &= 0 \end{aligned} \quad (1)$$

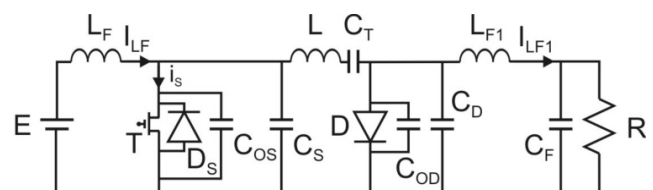


Fig. 1. ZVS Cuk MRC

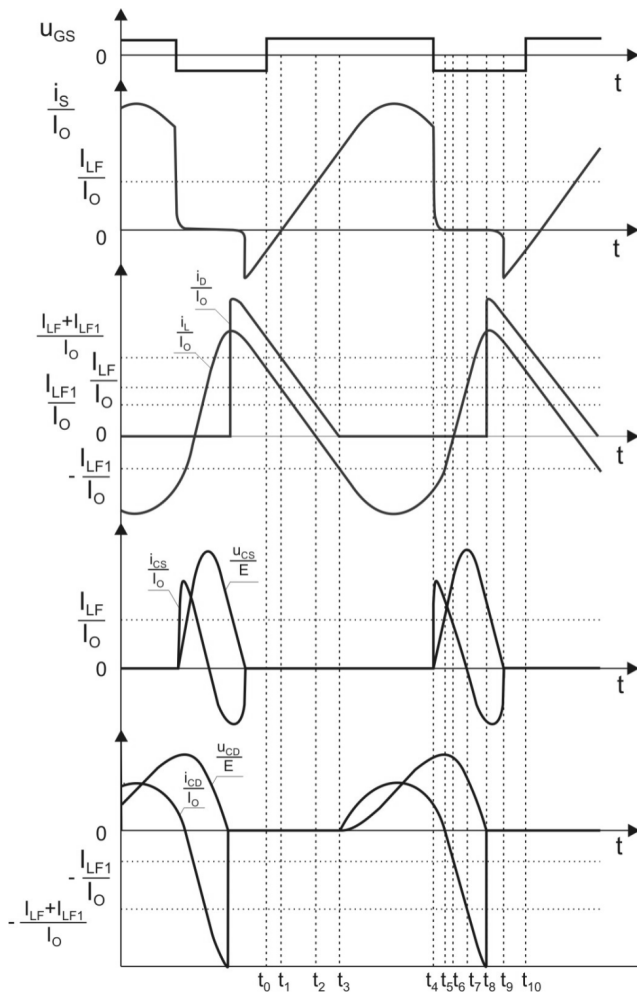


Fig. 2. Current and voltage waveforms in ZVS Cuk MRC (relative units)

where:

$u_{DS}$  — diode  $D_S$  forward voltage,

$u_D$  — diode  $D$  forward voltage.

In the second time interval ( $t_1 \leq t \leq t_3$ ) (Fig. 2), at  $t = t_1$ , current  $i_S = 0$ , the transistor starts to conduct at  $u_{CS} = 0$  (Fig. 3b). During this time interval,  $I_{LF}$  occurs in the circuit:  $E, L_F, R_T$  and  $E, L_F, L, C_T, D, I_{LF1}$  occurs in the circuit:  $D, (C_F \parallel R), L_{F1}$ . At  $t = t_2$ , current  $i_L = 0$ ,  $i_S = I_{LF}$  and  $i_D = -I_{LF1}$ . In the interval ( $t_2 \leq t \leq t_3$ ),  $i_L$  commutates with the current  $i_D$ .  $I_{LF}$  occurs in the circuit:  $E, L_F, R_T$ , and  $I_{LF1}$  is in circuits:  $L_{F1}, C_T, L, R_T, (C_F \parallel R)$  and  $L_{F1}, D, (C_F \parallel R)$ . At  $t = t_3$ ,  $i_D = 0$ ,  $D$  stops conducting. Voltages:  $u_{CS}$  and  $u_{CD}$  remain zero. The circuit in Figure 3b is described:

$$\begin{aligned} I_{LF} - i_S - i_L &= 0 \\ i_L - i_D - I_{LF1} &= 0 \\ i_L &= C_T \frac{du_{CT}}{dt} \\ L \frac{di_L}{dt} + u_{CT} + u_D - i_S R_T &= 0 \\ I_{LF1} - C_F \frac{dU_O}{dt} - \frac{U_O}{R} &= 0 \end{aligned} \quad (2)$$

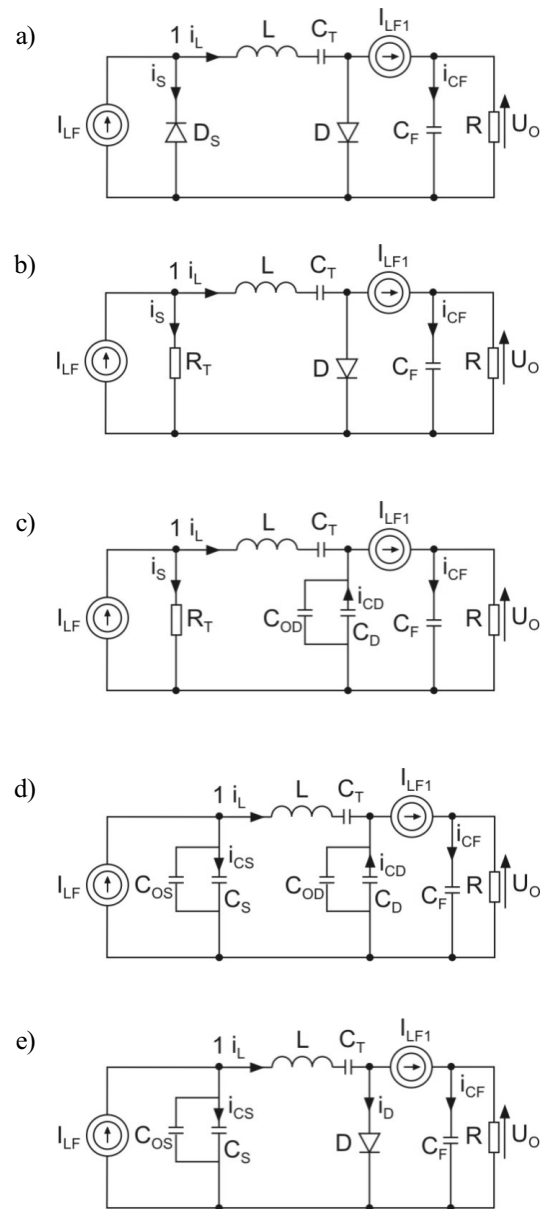


Fig. 3. Resonant circuit of ZVS Cuk MRC a) in the first interval, b) in the second interval, c) in the third interval, d) in the fourth interval, e) in the fifth interval

In the third time interval ( $t_3 \leq t \leq t_4$ ) (Fig. 2) the transistor is still on (Fig. 3c).  $i_L$  becomes greater than  $I_{LF1}$ , which initiates charging of  $C_D$  in the circuit:  $L, C_T, (C_D + C_{OD}), R_T$ .  $I_{LF}$  occurs in the circuit:  $E, L_F, R_T$ , and  $I_{LF1}$  is in:  $L_{F1}, C_T, L, R_T, (C_F \parallel R)$ . At  $t = t_4$  the transistor is turned off at  $u_{CS} = 0$ . The circuit in Figure 3c is described:

$$\begin{aligned} I_{LF} - i_S - i_L &= 0 \\ i_L + i_{CD} - I_{LF1} &= 0 \\ I_{LF1} - C_F \frac{dU_O}{dt} - \frac{U_O}{R} &= 0 \\ L \frac{di_L}{dt} + u_{CT} - i_S R_T - u_{CD} &= 0 \end{aligned} \quad (3)$$

$$\begin{aligned}
i_{CD} &= C_D \frac{du_{CD}}{dt} \\
i_L &= C_T \frac{du_{CT}}{dt}
\end{aligned} \quad (3)$$

In the fourth time interval ( $t_4 \leq t \leq t_8$ ) (Fig. 2), transistor  $T$  and diode  $D$  do not conduct (Fig. 3d). At  $t = t_4$ , transistor turn-off causes  $i_S$  to be commutated by  $i_{CS}$ . The resonant current  $i_L$  is a component of  $i_{CS}$  and occurs in the circuit:  $C_T$ ,  $L$ ,  $(C_S + C_{OS})$ ,  $(C_D + C_{OD})$ . In the time interval ( $t_4 \leq t \leq t_5$ ), energy accumulated in the inductance  $L$  charges capacitors  $C_S$  and  $C_D$ .  $I_{LF}$  occurs in the circuit:  $E$ ,  $L_F$ ,  $(C_S + C_{OS})$ , and  $I_{LF1}$  occurs in:  $L_{F1}$ ,  $C_T$ ,  $L$ ,  $(C_S + C_{OS})$ ,  $(C_{F1} \parallel R)$ . At  $t = t_5$ ,  $i_{CD} = 0$  and  $i_L = I_{LF1}$ . In the time interval ( $t_5 \leq t \leq t_6$ ), capacitor  $C_D$  starts to discharge. At  $t = t_6$ , current  $i_L = 0$  and  $i_{CD} = I_{LF1}$ . Energy stored in  $C_S$  and  $C_D$  forces a change in direction of the resonant current  $i_L$ .  $I_{LF}$  occurs in the circuits:  $E$ ,  $L_F$ ,  $(C_S + C_{OS})$  and  $E$ ,  $L_F$ ,  $L$ ,  $C_T$ ,  $(C_D + C_{OD})$ .  $I_{LF1}$  is in the circuit:  $L_{F1}$ ,  $(C_D + C_{OD})$ ,  $(C_{F1} \parallel R)$ . At  $t = t_7$ ,  $i_{CS} = 0$ ,  $i_L = I_{LF}$  and capacitor  $C_S$  starts to discharge. In the time interval ( $t_7 = t = t_8$ ),  $I_{LF}$  occurs in the circuit:  $E$ ,  $L_F$ ,  $L$ ,  $C_T$ ,  $(C_D + C_{OD})$ . The resonant current  $i_L$  occurs in the circuit:  $L$ ,  $C_T$ ,  $(C_D + C_{OD})$ ,  $(C_S + C_{OS})$ , and  $I_{LF1}$  is in:  $L_{F1}$ ,  $D$ ,  $(C_{F1} \parallel R)$ . At  $t = t_8$ ,  $u_{CD} = u_D$ . The circuit in Figure 3d is described:

$$\begin{aligned}
I_{LF} - i_{CS} - i_L &= 0 \\
i_L + i_{CD} - I_{LF1} &= 0 \\
I_{LF1} - C_F \frac{dU_O}{dt} - \frac{U_O}{R} &= 0 \\
i_L &= C_T \frac{du_{CT}}{dt} \\
i_{CS} &= C_S \frac{du_{CS}}{dt} \\
i_{CD} &= C_D \frac{du_{CD}}{dt} \\
u_{CT} + L \frac{di_L}{dt} - u_{CS} - u_{CD} &= 0
\end{aligned} \quad (4)$$

In the fifth time interval ( $t_8 \leq t \leq t_{10}$ ) (Fig. 2), at  $t = t_8$ , commutation of  $i_{CD}$  and  $i_D$  begins. Diode  $D$  is on. Owing to low value of junction capacitance  $C_{OD}$  of  $D$ , oscillations of  $i_D$  are negligible. Further discharging of capacitor  $C_S$  occurs in the circuit:  $L$ ,  $C_T$ ,  $D$ ,  $(C_S + C_{OS})$ .  $I_{LF}$  occurs in the circuit:  $E$ ,  $L_F$ ,  $L$ ,  $C_T$ ,  $D$ . At  $t = t_9$ , where  $u_{CS} = u_{DS}$ , diode  $D_S$  is ready to conduct  $i_S$ . Current  $i_{CS}$  of  $C_S$  is commutated by  $i_S$  of  $D_S$  (Fig. 3a). At  $t = t_{10}$  gate pulse to MOSFET initiates the next cycle of converter operation. The circuit in Figure 3e is described:

$$\begin{aligned}
I_{LF} + i_{CS} + i_L &= 0 \\
i_L - i_D - I_{LF1} &= 0
\end{aligned} \quad (5)$$

$$\begin{aligned}
I_{LF1} - C_F \frac{dU_O}{dt} - \frac{U_O}{R} &= 0 \\
u_{CT} + L \frac{di_L}{dt} - u_{CS} + u_D &= 0
\end{aligned}$$

$$i_L = C_T \frac{du_{CT}}{dt} \quad (5)$$

$$i_{CS} = C_S \frac{du_{CS}}{dt}$$

When the transistor is on, at high quality factor of the circuit, resonant frequency  $f_D$  of the circuit  $R$ ,  $L$ ,  $C_D$ ,  $C_{OD}$  is:

$$f_D = \frac{1}{2\pi\sqrt{L(C_D + C_{OD})}} \quad (6)$$

When the diode  $D$  is on, at high quality factor of the circuit, resonant frequency  $f_S$  of the circuit  $R$ ,  $L$ ,  $C_S$ ,  $C_{OS}$  is:

$$f_S = \frac{1}{2\pi\sqrt{L(C_S + C_{OS})}} \quad (7)$$

ZVS MRC is characterised by:

$$\begin{aligned}
f_N &= \frac{f}{f_S} \\
C_N &= \frac{C_D + C_{OD}}{C_S + C_{OS}} \\
M &= \frac{U_O}{E} \\
R_N &= \frac{R}{Z_S} \\
Z_S &= \sqrt{\frac{L}{(C_S + C_{OS})}}
\end{aligned} \quad (8)$$

where:

$f$  — operating frequency,  
 $f_N$  — operating frequency in relative units,  
 $C_N$  — ratio of capacitance,  
 $M$  — ratio of voltage conversion (output voltage in relative units),  
 $U_O$  — output voltage of the converter, ( $I_O$  — load current),  
 $R_N$  — load resistance in relative units,  
 $Z_S$  — characteristic impedance [1].  
 Input power  $P_{in}$  of the converter is:

$$P_{in} = I_{LF} * E \quad (9)$$

where:

$I_{LF}$  — mean value of current supply to the converter.

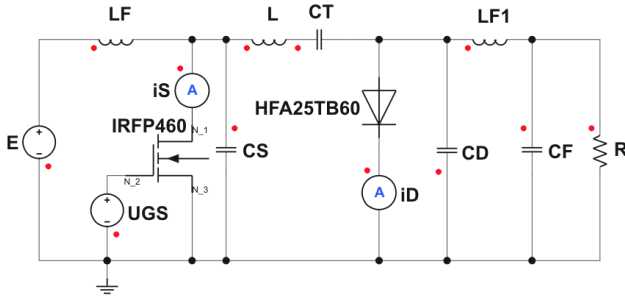


Fig. 4. Simulation model of ZVS Cuk MRC

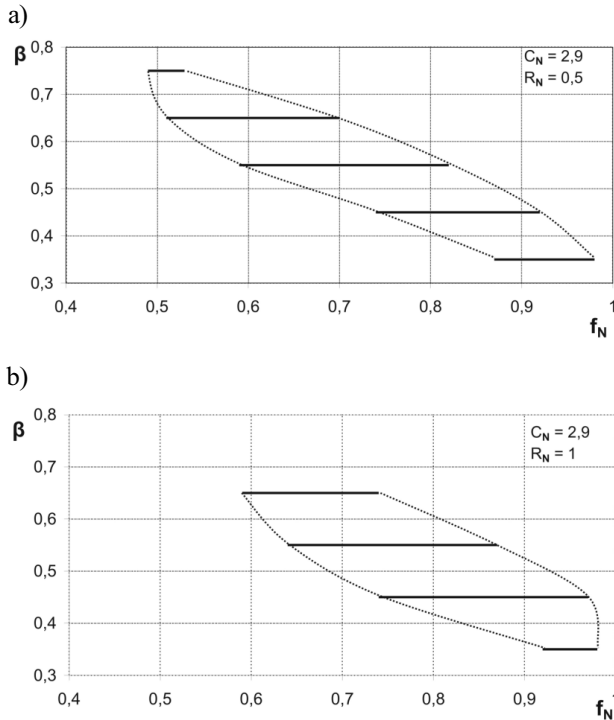


Fig. 5. ZVS operation area of Cuk MRC,  $C_N = 2.9$ , a)  $R_N = 0.5$ , b)  $R_N = 1$

Output power  $P_{out}$  of the converter is:

$$P_{out} = I_O * U_O = \frac{U_O^2}{R} \quad (10)$$

Efficiency  $\eta$  of the converter is:

$$\eta = \frac{P_{out}}{P_{in}} \quad (11)$$

The magnitudes defined by (8 ÷ 11) are necessary to determine control characteristics and efficiency  $\eta$  of the converter. Owing to complex mathematical apparatus, the characteristics and the efficiency  $\eta$  can be defined employing results of simulation testing.

#### 4. SIMULATION TESTING

ZVS Cuk MRC was subject to simulation testing with Simplorer programme. The simulation circuit in Figure 4 consists of MOSFET IRFP460 transistor (output capacitance

$C_{OS} = 870\text{pF}$ ) and HFA25TB60 fast recovery diode (junction capacitance  $C_{OD} = 100\text{pF}$ ) made by International Rectifier. The simulation model of Cuk MRC comprises:  $L = 7\mu\text{H}$ ,  $C_S = 7\text{nF}$ ,  $C_D = 23\text{nF}$ ,  $L_F = 600\mu\text{H}$ ,  $C_F = 10\mu\text{F}$ ,  $R = \text{variable}$ . Resonant frequencies:  $f_S = 678\text{kHz}$ ,  $f_D = 396\text{kHz}$ . Supply voltage  $E = 50\text{V DC}$ .

It was assumed that the converter employs ZVS technique. ZVS of the transistor is assured when transistor turns on as  $D_S$  is conducting at  $u_{CS} = 0$ . Transistor is always off when voltage  $u_{CS}$  is approximately zero. Turn-on of diode  $D$  is related to commutation of current  $i_{CD}$ , at  $u_{CD} = 0$ . The diode's turn-off occurs when  $i_{CD} = 0$  and  $u_{CD} = 0$ .

PWM technique was employed in the control system. Variation of operating frequency  $f$  and control modulation ratio  $\beta$  is then possible.

The ratio  $\beta$  is:

$$\beta = \frac{t_{on}}{T}$$

where:

$t_{on}$  — time, when transistor is on,  
 $T$  — period of transistor operation;  $T = \frac{1}{f}$

Results of simulation testing of the circuit served to determine ZVS operation area of the converter:  $\beta = f(f_N)$ , at  $R_N = 0.5$  and  $1$  (Fig. 5). The operation area defines permissible limits of frequency  $f_N$  and ratio  $\beta$  for which the criteria of ZVS are fulfilled. Frequency  $f_N$  reaches its minimum  $f_{Nmin}$  and maximum  $f_{Nmax}$  at  $\beta$  constant.

The range of operating frequency  $f_{Nmin} \leq f_N \leq f_{Nmax}$ , is variable depending on the values of  $\beta$  and  $R_N$ . Boundary frequencies  $f_{Nmin}$ ,  $f_{Nmax}$  tend to reduce as  $\beta$  rises.

Figure 6 illustrates selected current and voltage waveforms of ZVS Cuk MRC when  $f = 400\text{kHz}$  and  $\beta = 0.65$ . Transistor is turned on when diode  $D_S$  is conducting, at  $u_{CS} = 0$ .

Figure 7 presents control characteristics obtained in simulation testing:  $M = f(f_N)$ ,  $I_{Smax}/I_O = f(f_N)$ ,  $U_{CSmax}/E = f(f_N)$ ,  $U_{CDmax}/E = f(f_N)$  for the frequency range  $f_{Nmin} \leq f_N \leq f_{Nmax}$  and ratio  $\beta$  within the ZVS area of transistor's operation (Fig. 5). For  $C_N = 2.9$ ,  $R_N = 1$ , in the range  $0.59 \leq f_N \leq 0.98$  ( $400\text{kHz} \leq f \leq 667\text{kHz}$ ), the conversion ratio  $M$  is within:  $1.93 \geq M \geq 0.38$ , maximum voltage of the transistor  $U_{CSmax}/E$  is in the range:  $6.2 \geq U_{CSmax}/E \geq 3.0$ , maximum voltage of the diode  $U_{CDmax}/E$  is in the range:  $5.5 \geq U_{CDmax}/E \geq 1.1$ , maximum transistor current:  $5.44 \geq I_{Smax}/I_O \geq 6.22$ .

Figure 7 implies that increase of relative frequency  $f_N$  causes a drop in:  $M$ , and maximum voltages of: the transistor  $U_{CSmax}/E$  and diode  $U_{CDmax}/E$ .

Greater resistance  $R_N$  increases:  $M$ , maximum voltage of the diode  $U_{CDmax}/E$ , and maximum transistor current  $I_{Smax}/I_O$ . Values of maximum transistor voltage  $U_{CSmax}/E$  remain unchanged. Two inflexion points of characteristics occur in the waveforms  $I_{Smax}/I_O$ . The values of  $I_{Smax}/I_O$  are minimum for  $M = 1$ , and maximum for  $M = 0.5$ . The range of boundary values of relative frequency  $f_{Nmin}$  in control characteristics tends towards greater values as the value of  $R_N$  increases, and the range of boundary values of relative frequency  $f_{Nmax}$  remains unchanged.

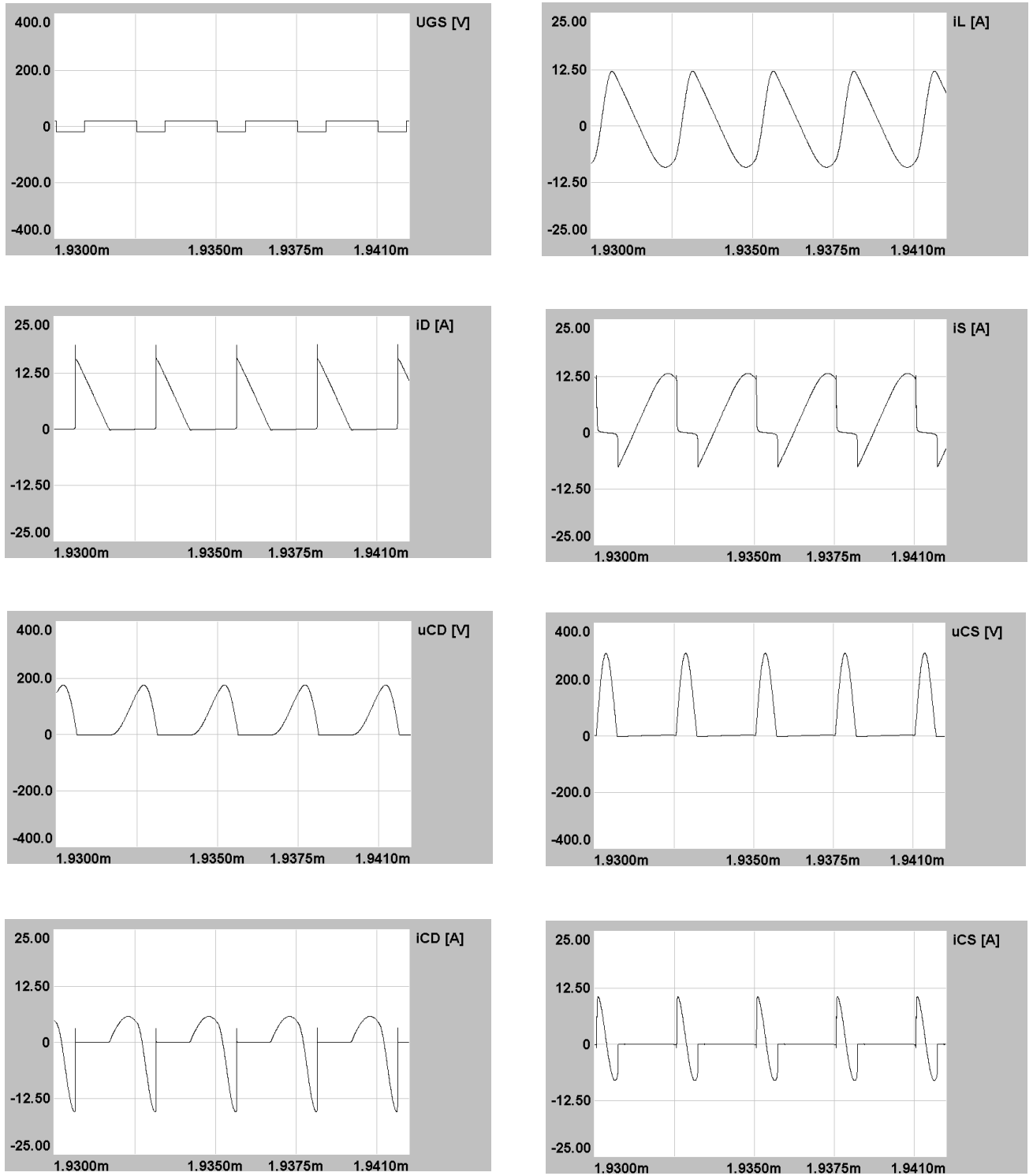


Fig. 6. Simulation current and voltage waveforms in ZVS Cuk MRC,  $C_N = 2.9$ ,  $R = 14.91\Omega$ ,  $U_O = 50.5V$ ,  $I_O = 3.4A$ ,  $f = 400kHz$  ( $f_N = 0.59$ ),  $\beta = 0.65$ ,  $\eta = 0.89$ ,  $P_{in} = 197W$ ,  $P_{out} = 175W$

Figure 8 illustrates total transistor power losses  $P_T$  and total diode  $D$  power losses  $P_D$ . Simulation testing results indicate that  $P_T$  are negligible ( $P_T < 10W$ ) in the frequency range  $0.62 \leq f_N \leq 0.9$  for  $R_N = 0.5$  and in  $0.68 \leq f_N \leq 0.95$  for  $R_N = 1$ . The increased resistance  $R_N$  causes higher  $P_T$  for the same  $f_N$ . Operation of  $T$  causes a major increase of  $P_T$  at  $\beta > 0.55$ .  $P_T$  rise by  $\Delta P_T = 30W$  in the range of frequency variation  $\Delta f_N = 0.15$ .

Power losses  $P_D$  of diode  $D$  reduce as  $R_N$  and  $f_N$  grow. The variation is approximately uniform throughout the

frequency range. The maximum losses  $P_D$  are about  $(5 \div 7)W$ .

In the ZVS operation of the converter, when frequencies  $f_N$  reduce,  $P_T$  are several times greater than  $P_D$  at the same  $\beta$  and  $R_N$ .

Both  $P_T$  and  $P_D$  significantly reduce as operating frequency of the circuit  $f_N$  grows. This results from lower transistor current  $i_S$  and diode current  $i_D$ , and from decrease of conduction losses in semiconductor elements in high frequency range. The resulting analysis indicates that the transistor should be characterized by the smallest possible resistance  $R_T$ .

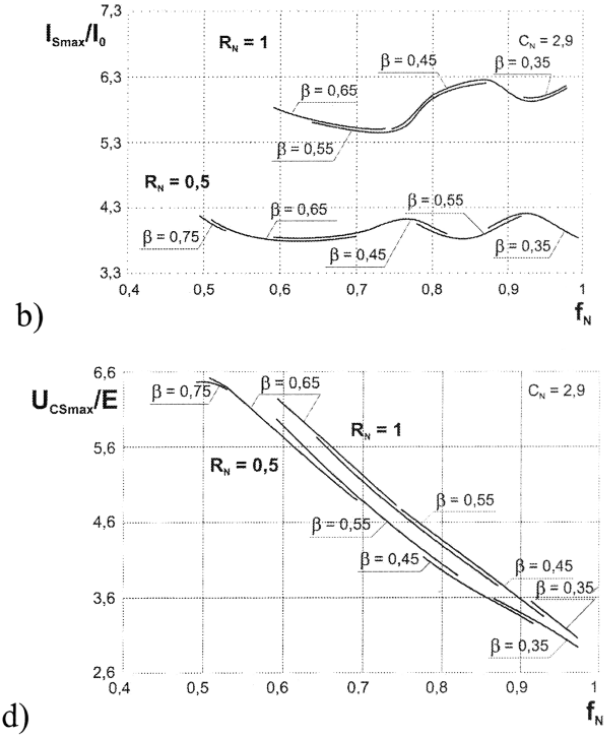
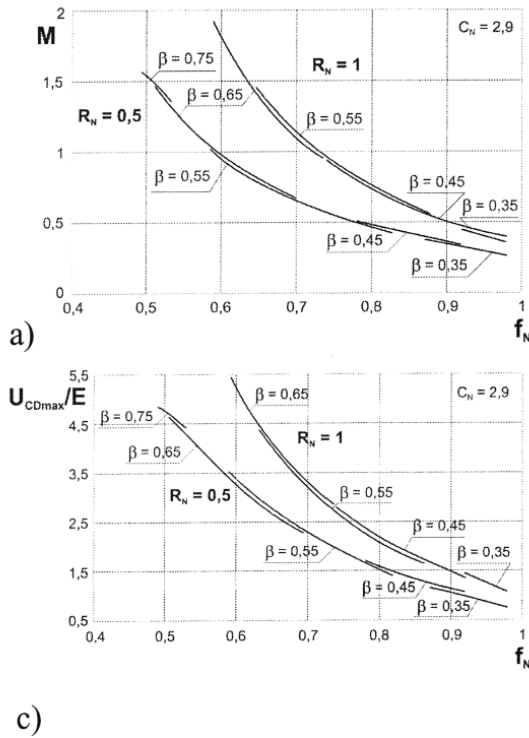


Fig. 7. Control characteristics for ZVS Cuk MRC in relative units,  $C_N = 2.9$ ,  $R_N = 0.5$ ,  $R_N = 1$ ; a) conversion ratio  $M$ ; b) maximum transistor current  $I_{Smax}/I_0$ ; c) maximum diode voltage  $U_{CDmax}/E$ ; d) maximum transistor voltage  $U_{CSmax}/E$

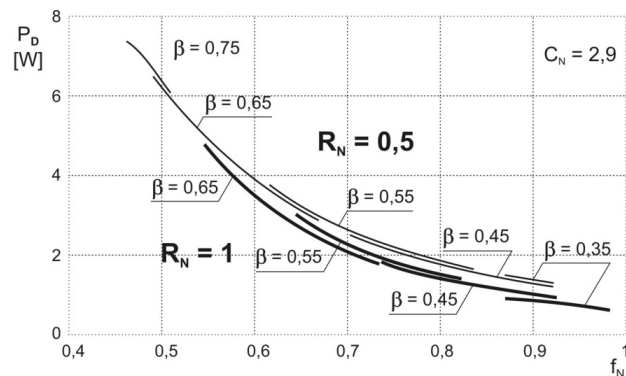
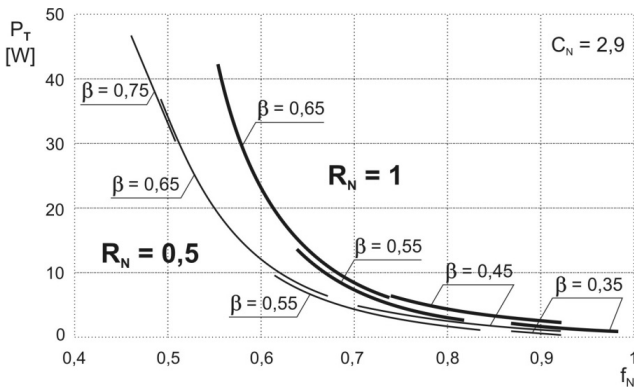


Fig. 8. a) Total transistor power losses  $P_T$ ; b) total diode  $D$  power losses  $P_D$

Figure 9 shows the output power  $P_{out}$  of ZVS Cuk MRC. Increased  $R_N$  causes a power  $P_{out}$  increase at the same frequency  $f_N$ . For  $\beta > 0.55$ ,  $P_{out}$  grows significantly in low frequency range.

Figure 10 shows efficiency  $\eta$  of ZVS Cuk MRC. The converter's efficiency is within the range  $0.86 = \eta = 0.92$  at  $R_N$ . Greater  $f_N$  does not alter  $\eta$  significantly at  $C_N = \text{const}$ ,  $R_N = \text{const}$ . For reducing  $f_N$ , particularly at  $\beta > 0.55$ ,  $\eta$  drops slightly as losses  $P_T$  climb dynamically. Great and constant  $\eta$  can be maintained when  $f_N$  is decreasing since output power  $P_{out}$  increases dynamically at the time (Fig. 9).

## 5. CONCLUSION

On the basis of simulation testing of MRC under analysis, it can be concluded that:

1. ZVS Cuk converter provides good conditions of zero-voltage switching for both the transistor and the diode. The area of ZVS operation is determined by switching frequency and ratio of modulation, and depends on load resistance.
2. Maximum voltages of transistor and diode decrease as the converter's operating frequency increases or load resistance reduces.
3. Energy efficiency of ZVS Cuk MRC is great and depends primarily on conduction losses in semiconductor elements.

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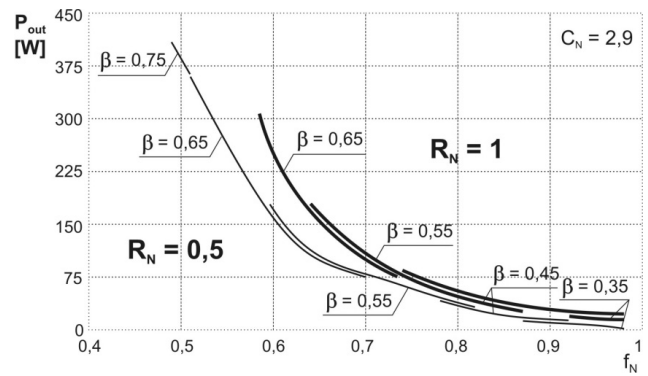


Fig. 9. Output power  $P_{out}$  of ZVS Cuk MRC

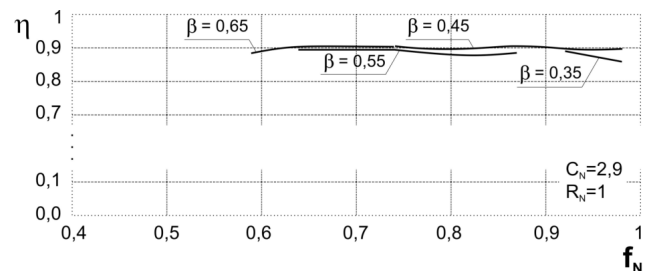
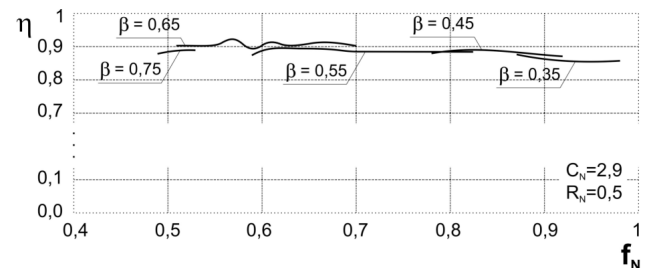


Fig. 10. Efficiency  $\eta$  of ZVS Cuk MRC,  $C_N = 2.9$ ; a)  $R_N = 0.5$ ; b)  $R_N = 1$