Classical Control of the Neutral Point in 4-wire 3-phase DC-AC Converters

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Summary: In this paper, the classical control techniques are applied to the neutral point in a 3-phase 4-wire DC-AC power converter. The converter is intended to be connected to 3-phase 4-wire loads and/or the power grid. The neutral point can be steadily regulated by a simple controller, involving in voltage and current feedback, even when the three-phase converter system (mostly, the load) is extremely unbalanced. The achievable performance is analyzed quantitatively and the parameters of the neutral leg are determined. Simulations show that the proposed theory is very effective.

1. INTRODUCTION

For various reasons, there is today a proliferation of small power generating units which are connected to the power grid at the low-voltage end. Some of these units use synchronous generators, but most use DC or variable frequency generators coupled with electronic power converters. For example, wind-turbines are most effective if free to generate at variable frequency, so they need AC (variable frequency) to DC and then to AC (50Hz) conversion [1]; small gas-turbine driven generators operate at high frequencies and so they also require AC-DC-AC conversion [2]; photo-voltaic arrays require DC-AC conversion [3]. In these (low-voltage grid connected) systems, a neutral line is usually needed to provide a current path for possible unbalanced loads. If the neutral point is not well controlled, the neutral current usually makes the neutral point shift. The shift of the neutral point may result in unbalanced/variable output voltage, DC component in the output, larger neutral current or even more serious problems. Hence, how to generate a stable neutral point efficiently and simply has now become a very important problem and will become more important in the future when industrial applications increase. Although 3-phase 3-wire electronic power converters have been widely studied in recent years [4, 5], 3-phase converters with a neutral line have been discussed only in few papers [6, 7].

There are three circuit topologies available to generate a neutral point [8]. One is a split DC link, as shown in Figure I(a). The neutral point is clamped at half of the DC link voltage. This is the simplest topology. However, since the neutral current flows through the capacitors, unrealistically high capacitance is needed if the load unbalance is severe. Another drawback is that the neutral point usually shifts and becomes non-neutral in reality. As a result, this topology is actually not used in DC-AC converters which supply power to loads and/or grid, although it is widely used in active power filters [9, 10]. A better way to handle the neutral point is to add an additional fourth leg, called a neutral leg, to the conventional three-leg converter [6], as shown in Figure I(b). The space vector modulation control [7] for this topology is available. Comparing this topology to the split DC link, the neutral point is more stable and the output voltage is about 15% higher (using the same DC link voltage). However, the additional neutral leg cannot be independently controlled to maintain the neutral point and, hence, the corresponding control design (including the PWM waveform generating

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Fig. 1. Circuit topologies to generate a neutral point in DC-AC converters
scheme) becomes much more complicated, as pointed out in [7]. The third one is the combination of the split DC link and the neutral leg, as shown in Figure 1(c). The control of the neutral point is decoupled from the control of the three-phase converter. A simplified linear model of this circuit has been built in [8] and a controller is designed with the advanced $H^\infty$ control theory there. In this paper, the system is further analyzed and a controller is designed using the classical control theory. Insightful understanding of the circuit is provided.

2. MODELING OF THE CIRCUIT

The linear model of the system developed here is slightly different from that in [8] because of ignoring the resistance of the inductor and assuming that the capacitors are the same. As a result, some more insightful understanding can be obtained.

Assume the voltages across the capacitors $C_N$ with respect to the neutral point $N$ are $V_+$ and $V_-$, respectively. Then the DC link voltage is:

$$V_{DC} = V_+ - V_-$$

and the shift of the neutral point is$^1$:

$$\varepsilon = V_+ + V_-$$

According to the Kirchhoff’s laws, the following equations are satisfied:

$$\begin{align*}
  u_N &= L_N \frac{di_L}{dt} \\
  i_N &= i_L + i_c \\
  i_c &= C_N \frac{dV_+}{dt} + C_N \frac{dV_-}{dt} = C_N \frac{d\varepsilon}{dt}
\end{align*}$$

Assume the average of the firing pulse during a switching period is $p$ (with the magnitude of $\pm 1$), as shown in Figure 2, then the duty cycle of the firing pulse is:

$$d = \frac{1+p}{2}$$

Fig. 2. The firing pulse $p$ and the inductor voltage $u_N$

and the average of the output voltage $u_N$ (i.e. the inductor voltage), as shown in Figure 2, is:

$$u_N = dV_+ + (1-d)V_- = \frac{1+p}{2} V_+ + \frac{1-p}{2} V_- \quad (2)$$

Combining the Laplace transformation of (1) and (2), the block diagram of the neutral leg can be obtained as shown in Figure 3.

The amplifying effect of the IGBT bridge (the block $\frac{V_{DC}}{2}$ in Figure 3) can be canceled/scalld by $\frac{2}{V_{DC}}$ in the controller to be designed and, hence, ignoring this block does not affect the control design. Moreover, the block $\frac{1}{2}$ in Figure 3 can be canceled by the proportional gain of the controller to be designed because the setpoint for the shift $\varepsilon$ is 0. Based on these two facts, the problem is equivalently changed from controlling the average $p$ of the firing pulse, as shown in Figure 3, to controlling the voltage $u_N$, as shown in Figure 4. As can be seen later, the proportional gain from the shift $\varepsilon$ to $u_N$ is designed to be much larger than $\frac{1}{2}$. Hence, when implementing the controller, this block is usually ignored and only the scaling block $\frac{2}{V_{DC}}$ is needed to cascade to the designed controller.

According to (1):

$$\varepsilon = \int_0^t \frac{1}{C_N} (i_N - i_L) \, dt \quad (3)$$

Since the control objective is to maintain the point $N$ as a neutral point (i.e. the shift $\varepsilon = 0$), then:

$$\int_0^t (i_N - i_L) \, dt = C_N \varepsilon (t)$$

is expected to be very close to 0 all the time. As a result, $i_c$ is expected to be almost equal to $i_N$. This means the majority of the neutral current should flow through the inductor $L_N$ but not through the capacitors $C_N$. The smaller the $i_c$ the smaller

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1) Actually, $\varepsilon$ is twice the shift of the neutral point with respect to the mid-point of the DC link. In order to simplify the exposition, it is called the shift.
the shift \( \varepsilon \). Hence, the capacitors are not necessarily very large like those in the conventional split DC link topology. This is a very important fact.

In this paper, we try to design a controller as simple as possible, which is cost-effective and easy to be implemented. A more mathematical controller is designed in [8] based on the \( H^\infty \) control theory.

3. CONTROLLER DESIGN

The system shown in Figure 4 is a double integrator system, which is difficult to control in engineering. A proportional-integral (PI) controller or even a proportional (P) controller cannot stabilize it. A possible controller to be able to stabilize the system is a lead-lag compensator:

\[
C(s) = K_c \frac{bs + 1}{as + 1}
\]

where \( K_c > 0 \) and \( b > a > 0 \) with the measurement of \( \varepsilon \). This control scheme will not be further discussed here. Instead, a voltage-current control scheme will be proposed.

The proposed voltage-current control scheme is shown in Fig. 5 based on the fact that the smaller the current \( i_c \) the smaller the shift \( \varepsilon \). An inner current loop is introduced to attenuate the effect of the neutral current \( i_N \) on the current \( i_c \) and an outer voltage loop is used to regulate the shift \( \varepsilon \). Because there exists an integrator in both the voltage loop and the current loop, the two loop controllers can be simply designed as proportional controllers \( K_v \) and \( K_i \) respectively. In this control scheme, one voltage \( \varepsilon \) and one current \( i_c \) are measured for feedback.

3.1. Design of the current controller \( K_i \)

The objective of the current loop is to attenuate the effect of neutral current \( i_N \) on \( i_c \), as much as possible, at least for those frequency components under consideration. In our application, the fundamental frequency is 50Hz and the highest frequency components under consideration is up to the 31st harmonics, i.e., 1550Hz. Approximately, the corresponding angular frequency is 10000rad/sec. As can be seen later, this is a crucial parameter for the performance of the neutral point (the level of the shift \( \varepsilon \)).

The transfer function from \( i_N \) to \( i_c \) in Figure 6(a) is:

\[
\frac{sL_N}{sL_N + K_i}
\]

The Bode plot is shown in Figure 6(b). The corner angular frequency, called the inner loop (angular) frequency, is \( \omega_i = \frac{K_i}{L_N} \). As shown in Section 2, the smaller the current \( i_c \), the smaller the shift \( \varepsilon \). In order to make \( i_c \) as small as possible, the inner loop frequency \( \omega_i \) should be high enough while considering the physical limit\(^1\). Hence, the current-loop control parameter is:

\[
K_i = \omega_i L_N \quad (4)
\]

Here, \( \omega_i \) is chosen as 10000rad/sec. Accordingly, the switching frequency \( f_s \) is chosen as 10kHz, which is larger than 3~4 times of 1550Hz.

3.2. Design of the voltage controller \( K_v \)

After the current loop is designed, the system shown in Figure 5 is equivalent to the one shown in Figure 7, based on which the voltage controller \( K_v \) will be designed. The transfer function from \( i_N \) to \( \varepsilon \) is:

\[
T = \frac{sL_N}{s^2 L_N C_N + sK_i C_N + K_v} \quad (5)
\]

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1) As can be seen later in Figure 9, the larger the \( \omega_i \), the higher the high frequency gain from \( i_N \) to \( u_N \) is required. But this is usually limited by the low-pass filtering effect of the system.
and its magnitude frequency response is:

\[
|T(j\omega)| = \frac{\omega L_N}{\sqrt{\left(\frac{K_u - \omega^2 L_N C_N}{\omega} \right)^2 + \left(\omega K C_N\right)^2}} = \frac{\left(\frac{K_u}{\omega} - \omega L_N C_N\right)^2}{\left(\frac{K_u}{\omega} - \omega L_N C_N\right)^2 + (K C_N)^2}
\]

which achieves its maximal value when:

\[
\frac{K_u}{\omega} - \omega L_N C_N = 0
\]

The corresponding frequency is called outer loop (natural angular) frequency and denoted as \(\omega_{o_o}\) i.e.,

\[
\omega_o = \sqrt{\frac{K_u}{L_N C_N}}
\]

or:

\[
K_u = \omega_o^2 L_N C_N
\]

If the voltage controller \(K_u\) is tuned according to this formula, then the transfer function (5) becomes:

\[
T = \frac{s}{s^2 + s \omega_o + \omega_o^2} \frac{1}{C_N}
\]

The Bode plot is shown in Figure 8 for different \(\omega_o\). The Bode plot consists of three parts A, B and C. When \(K_u\) or \(\omega_o\) is increased, the left part A moves towards right while the length of the middle part B is shortened and the right part C remains almost unchanged (when \(K_u\) or \(\omega_o\) is not extremely large), and the shift \(\epsilon\) becomes smaller. When \(C_N\) is decreased, parts B and C move up and part A extends while the length of part B is shortened, and the shift \(\epsilon\) becomes larger. Hence, in order to reduce the shift \(\epsilon\), larger \(K_u\) (or \(\omega_o\)) and larger \(C_N\) are needed. Moreover, the left part A of the Bode plot should move towards right as close as possible to the right part C. The extreme case is to choose:

\[
\omega_o = \omega_j
\]

This makes use of the full physical capability of the controller. In this case, the corresponding Bode plot is shown as the thick line in Figure 8 and the voltage controller is then obtained as:

\[
K_u = \omega_j^2 L_N C_N
\]
As is well known, any periodic neutral current: be decomposed as a series:

\[ i_N = \sum_{j=0}^{\infty} I_j \sin \left( 2\pi f t + \phi_j \right) \]  

(11)

where \( f \) is the fundamental frequency. In engineering, only a few components needs to be considered. Here, we consider the first 31 harmonic components, bearing in mind that the DC component does not contribute to the shift according to (10). Hence, the root-mean-square value of the shift is:

\[ E = \sqrt{\frac{1}{2} \sum_{j=1}^{31} E_j^2} \]

\[ = \sqrt{\frac{2}{\pi} \sum_{j=1}^{31} \left( \frac{j\pi f I_j}{\omega_j^2 C_N} \right)^2} \]

\[ = \frac{\pi f}{\omega_f^2 C_N} \sqrt{\sum_{j=1}^{31} 2j^2 I_j^2} \]

Another important issue in engineering is how the control signal \( u_N \) behaves. The transfer function from \( i_N \) to \( u_N \) is:

\[ T_u = \frac{sL_N (sK_C + K_v)}{s^2 L_N C_N + sK_C + K_v} \]

\[ = \frac{sL_N (s\omega_o + \omega_o^2)}{s^2 + s\omega_o + \omega_o^2} \]  

(12)

Moreover, when \( \omega_o = \omega_f \):

\[ T_u = \frac{s(s + \omega_f)}{s^2 + s\omega_f + \omega_f^2} \omega_f L_N \]

The Bode plot is shown in Figure 9. There is a small peak of about 3dB near \( \omega_o \). This does not cause a large control signal \( u_N \). In the frequency range under consideration, the control signal can be calculated as:

\[ u_N = 2\pi f_N L_N I_N \]  

(13)

where \( f_N \) is the frequency of the neutral current \( i_N \) with a peak value of \( I_N \) (assuming there is only one frequency component to simplify the exposition). This coincides with the analysis in Section 2. It means that for a given system the allowable high frequency neutral current decreases when the frequency increases. The Bode plot with \( \omega_o = \frac{1}{2} \omega_f \), corresponding to the case when the two poles of the closed-loop system are identical and \( K_v = \frac{1}{4} \omega_f^2 L_N C_N \) is also shown in Figure 9.

There is no peak anywhere, but as shown in (9) the shift will be doubled and, as can be seen later, the capacitor needed will be doubled, too. Hence, it is worth using \( \omega_o = \omega_f \).

4.2. Design of the neutral leg

4.2.1. The capacitor \( C_N \)

The capacitor \( C_N \) can be designed, according to (9), as:

\[ C_N \geq \frac{2\pi f I_N}{\omega_o \omega_o E_m} \]  

(14)

where \( I_N \) is the maximal peak value of the main component of the neutral current \( i_N \), \( f \) is the frequency of the main component of \( i_N \), \( \omega_f \) is the inner loop frequency, \( \omega_o \) is the outer loop frequency and \( E_m \) is the desired maximal ripple voltage.

If the other components in the neutral current form a large portion of \( i_N \), a conservative design is to add all the capacitances for the different components together and then verify if the achievable shift meets the requirement.

**Example:** Assume the neutral current is \( I_N = 100A \) (peak) at \( f = 50Hz \) and \( \omega_f = \omega_o = 10000rad/sec \). If the desired maximal shift is 1V, then \( C_N \geq 314\mu F \). This capacitance is very small.

4.2.2. The inductor \( L_N \)

The equation (9) shows that the inductor does not affect the shift (when the control signal \( u_N \) is not limited). However, it does affect the shift when the neutral current are too large and the neutral leg cannot supply the required voltage.

As discussed in Section 2, the current \( i_N \) needs to be almost equal to the neutral current \( i_N \). Hence, for a sinusoidal neutral current \( i_N \) with a specific frequency component \( f \) (of which the peak value is \( I_N \)), the control signal \( u_N \) is required to be:

\[ u_N = 2\pi f L_N I_N \]

This has been verified in (13). Assume the possible peak voltage of \( u_N \) is about \( \frac{k}{2} V_{DC} \) (\( k \) is a constant coefficient, which may often be 0.8 ~ 1 depending on the PWM waveform generating scheme and \( V_{DC} \) is the DC link voltage), then:

\[ L_N \leq \frac{k}{4\pi f I_N} V_{DC} \]  

(15)
This formula can also be used to verify if the inductor $L_N$ makes the control signal $u_N$ constrained by the DC link voltage. Since a larger inductor does not improve the shift, a small inductor is desired because a smaller inductor is more cost-effective and it allows higher neutral current with higher frequency (when $V_{DC}$ is the same). However, a too small inductor results in very large surge current flowing through the switches. Hence, the inductor $L_N$ should be designed with more consideration on this point, i.e.

$$L_N \geq \frac{1}{2} \frac{V_{DC}}{\delta_m}$$

where $\delta_m$ is the maximum allowable $\frac{di}{dt}$ of the switches. Usually, 0.1mH is quite enough [11]. An extreme condition is that the current flowing through the inductor is a triangle waveform with a frequency equal to the switching frequency $f_s$. Then the following condition should be met:

$$L_N \geq \frac{V_{DC}}{8I_m f_s}$$  \hspace{1cm} (16)

where $I_m$ is the maximum allowable current of the switch. Usually, this condition is stronger than the previous one and the inductor is chosen according to (15) and (16), i.e.

$$\frac{V_{DC}}{8I_m f_s} \leq L_N \leq \frac{k V_{DC}}{4\pi f I_N}$$

Another factor which should be taken into account is that a too small $u_N$ means an insufficient control effect. Hence, if the neutral current is normally large then a small inductor is desired; if the neutral current is normally small then a larger inductor is required.

5. SIMULATION RESULTS

In the following simulations, a single phase buck converter is used to simulate the neutral current $i_N$ of a three-phase converter. The fundamental frequency of this buck converter can be set at different frequencies to simulate different harmonic components in a neutral line. The parameters of the neutral leg used in these simulations are $L_N = 10\text{mH}$, $C_N = 4000\mu\text{F}$, $V_{DC_e} = 900\text{V}$ and $f_s = 10\text{kHz}$. The controller is designed as $K_i = 100$ and $K_p = 4000$ (i.e. $\omega_i = \omega_p = 10000\text{rad/sec}$).

In order to see the signals clearly, the signals $i_N$ and $u_N$ are filtered by a hold filter:

$$F(s) = \left(1 - e^{-\frac{s}{f_s}}\right)s$$

This is a notch filter of which the notchting frequencies are the switching frequency $f_s$ and its integer multiples. Hence, the effect of the switching frequency is eliminated (note that this may change the corresponding waveforms).

Simulations are done for cases with different $i_N$:

1. ideally balanced load ($i_N = 0$).
   This is an ideal situation. The simulation results are shown in Figure 10. The peak value of the shift is less than 0.01V; the duty cycle of the firing pulse $p$ is about 50% and $u_N$ is about 0V although there are some pulses left after filtered by the hold filter; the current flowing through the inductor is nearly a triangle wave with an amplitude of about 1.25A; the current $i_e$ is very small although there are some spikes (not shown in the figure because of the filtering effect of $F$). The average of the inductor current is 0, which is the same as the neutral current.

2. $50\text{Hz}$ neutral current
   Assume the buck converter has a single phase load $R = 5\Omega$ in series with an inductor $L = 5\text{mH}$ and works at 50 Hz (the fundamental component of the output voltage is 360V peak). This offers a neutral current of about 68 A peak. The simulation results are shown in Figure 11. The peak value of the shift is less than 0.1 V; the inductor current is almost the same as the neutral current and the current $i_e$ is very small. The neutral leg provides a voltage of about 200V peak.
Fig. 11. Simulation results when the main component of the neutral current is 68 A, 50Hz

(3). ISOHz neutral current

Assume the buck converter has a single phase load \( R = 10\Omega \) in series with an inductor \( L = 5\text{mH} \) and works at 150 Hz (the fundamental component of the output voltage is 360V peak). This offers a neutral current of about 34 A peak at 150Hz. The simulation results are shown in Figure 12. The peak value of the shift is about 0.1 V; the inductor current is almost the same as the neutral current and the current \( i_c \) is very small. The neutral leg provides a voltage of about 300V peak.

(4). DC neutral current

When the single-phase converter works at 0Hz with an output voltage of 360V and the load is \( R = 5\Omega \), the neutral line current is about 72A. The simulation results are shown in Figure 13. The shift is almost 0 when the neutral current is stable.

6. CONCLUSIONS

There are many frequency-related parameters involved in this paper. A summary is given in Table 1.

In this paper, a control strategy is proposed for a topology consisting of a conventional neutral leg and a split DC link to generate a stable neutral point. The conventional neutral leg provides a path for the neutral current and charges/discharges the capacitors to maintain the neutral point; the capacitors provide a way to independently control the conventional neutral leg and the 3-phase converter. The role of the capacitors has been changed from maintaining the neutral point to providing a way for control. As a matter of fact, only one capacitor is necessary. This results in an unsymmetric topology but does not change the control design.

<table>
<thead>
<tr>
<th>frequency</th>
<th>value</th>
</tr>
</thead>
<tbody>
<tr>
<td>fundamental frequency ( f )</td>
<td>50Hz</td>
</tr>
<tr>
<td>harmonics up to 31st</td>
<td>100 – 1550Hz</td>
</tr>
<tr>
<td>outer loop frequency ( \omega_o )</td>
<td>10000rad/sec</td>
</tr>
<tr>
<td>inner loop frequency ( \omega_i )</td>
<td>10000rad/sec</td>
</tr>
<tr>
<td>switching frequency ( f_s )</td>
<td>10kHz</td>
</tr>
</tbody>
</table>

Table 1. Frequency-related parameters
much. The controller designed here is very simple and easy to implement. Many simulations have shown that the designed system is effective in generating a stable neutral point, even when the 3-phase system is severely unbalanced and the neutral current is very large.

Some problems are not discussed here, for example, the inequality of the capacitors (which is often the case in reality), the effect of the inconstant DC link voltage \( V_{DC} \), the effect of the loads of the 3-phase converter on the neutral leg and the coupling effects among them etc. Some of the problems are tackled in [8], but some needs to be further studied.

REFERENCES


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